REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R167-96.	96-07-01	M. A. Frye
B	Changes in accordance with NOR 5962-R126-97.	96-11-19	M. A. Frye
C	Add device type 03. Add vendor CAGE 01295 as source of supply for device type 03. Update boilerplate. Editorial changes throughout.	97-03-26	R. Monnin
D	Boilerplate update and part of five year review. tcr	06-05-05	R. Monnin
E	Update drawing to reflect current MIL-PRF-38535 requirements. - llb	14-10-07	Charles F. Saffle

REV	E	E	E	E	E	E	E	E	E	E	E	E	E							
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47							
REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
REV STATUS			REV			E	E	E	E	E	E	E	E	E	E	E	E	E	E	
OF SHEETS			SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

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CHECKED BY
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APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
95-05-12

REVISION LEVEL
E

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

MICROCIRCUIT, DIGITAL, MEMORY, DIGITAL, CMOS, 256K X 16 MULTIPORT VIDEO RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-94549**

SHEET 1 OF 47

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	-	94549	01	Q	X	A
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)
___ Drawing number ___/						

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01	55161	256K x 16-bit multiport video RAM	80 ns
02	55161	256K x 16-bit multiport video RAM	70 ns
03	55161	256K x 16-bit multiport video RAM	75 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA1-68	68	Pin grid array
Y	See figure 1	64	Flatpack with tie bar

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 (see 6.6.1 herein).

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range (V_{CC})	-1.0 V dc to +7.0 V dc
Input voltage range	-1.0 V dc to +7.0 V dc
DC short circuit output current	50 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.1 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X	See MIL-STD-1835
Case Y	15°C/W
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Supply voltage (V_{SS})	0 V
Input high voltage (V_{IH})	2.4 V dc minimum to 6.5 V dc maximum
Input low voltage (V_{IL})	-1 V dc minimum to 0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201-2107.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ All voltage values in this specification are with respect to V_{SS}.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime’s agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 041 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limit		Unit
						Min	Max	
Input leakage current	I_{LI}	$0.0\ V \le V_{IN} \le 5.8\ V$, All other pins at 0 V to V_{CC}, $V_{CC} = 5.5\ V$		1,2,3	All	-10	+10	μA
Output leakage current 2/	I_{LO}	$\overline{OE} \ge V_{IH}$, $0.0 \le V_{OUT} \le V_{CC}$ $V_{CC} = 5.5\ V$		1,2,3	All	-10	+10	μA
Output high voltage	V_{OH}	$I_{OH} = -1$ mA		1,2,3	All	2.4		V
Output low voltage	V_{OL}	$I_{OL} = 2$ mA		1,2,3	All		0.4	V
Operating supply current 4/	I_{CC1}	3/	SAM port standby	1,2,3	01		160	mA
					02,03		165	
	I_{CC1A}	$t_{c(SC)}$ = Min	SAM port active		01		195	
					02,03		210	
Standby supply current	I_{CC2}	All clocks = V_{CC}	SAM port standby	1,2,3	All		12	mA
	I_{CC2A}	$t_{c(SC)}$ = Min	SAM port active		01		65	
					02,03		70	
$\overline{RAS}$ -only refresh supply current	I_{CC3}	3/	SAM port standby	1,2,3	01		160	mA
					02,03		165	
	I_{CC3A}	$t_{c(SC)}$ = Min 3/	SAM port active		01		195	
					02,03		215	
Page-mode supply current 4/	I_{CC4}	$t_{c(P)}$ = Min 5/	SAM port standby	1,2,3	01		95	mA
					02,03		100	
	I_{CC4A}	$t_{c(SC)}$ = Min 5/	SAM port active		01		130	
					02,03		145	
$\overline{CAS}$ -before- $\overline{RAS}$ supply current	I_{CC5}	3/	SAM port standby	1,2,3	01		160	mA
					02,03		165	
	I_{CC5A}	$t_{c(SC)}$ = Min 3/	SAM port active		01		195	
					02,03		210	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol/ altern. symbol	Conditions 1/ $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit Min	Max	Unit
Data-transfer supply current	I_{CC6}	3/ SAM port standby	1,2,3	01		170	mA
				02,03		180	
	I_{CC6A}	$t_{c(SC)}$ = Min SAM port active		01		200	
				02,03		225	
Input capacitance 6/	C_{IN}	f = 1.0 MHz, T_A = +25°C, see 4.4.1e	4	All		10	pF
Output capacitance, SQ and DQ 6/	C_{OUT1}	f = 1.0 MHz, T_A = +25°C, see 4.4.1e	4	All		15	pF
Output capacitance, QSF 6/	C_{OUT2}	f = 1.0 MHz, T_A = +25°C, see 4.4.1e	4	All		12	pF
Functional tests		See 4.4.1c	7,8A,8B	All			
Access time from $\overline{CAS}$	$t_{a(C)}$ t_{CAC}	$t_{d(RLCL)}$ = Max, See figure 4 7/	9,10,11	All		20	ns
Access time from column address	$t_{a(CA)}$ t_{AA}	$t_{d(RLCL)}$ = Max See figure 4 7/	9,10,11	01		40	ns
				02		35	
				03		38	
Access time from $\overline{CAS}$ high	$t_{a(CP)}$ t_{CPA}	$t_{d(RLCL)}$ = Max See figure 4 7/	9,10,11	01		45	ns
				02		40	
				03		43	
Access time from $\overline{RAS}$	$t_{a(R)}$ t_{RAC}	$t_{d(RLCL)}$ = Max See figure 4 7/	9,10,11	01		80	ns
				02		70	
				03		75	
Access time of DQ from $\overline{TRG}$ low	$t_{a(G)}$ t_{OEA}	See figure 4 7/	9,10,11	All		20	ns
Access time of SQ from SC high	$t_{a(SQ)}$ t_{SCA}	See figure 4 C_L = 30 pF 7/	9,10,11	01		25	ns
				02		20	
				03		23	
Access time of SQ from $\overline{SE}$ low	$t_{a(SE)}$ t_{SEA}	See figure 4 C_L = 30 pF 7/	9,10,11	01		20	ns
				02		15	
				03		18	
Disable time, random output from $\overline{CAS}$ high 8/	$t_{dis(CH)}$ t_{OFF}	See figure 4, C_L = 50 pF 7/	9,10,11	All	0	20	ns
Disable time, random output from $\overline{RAS}$ high 8/	$t_{dis(RH)}$	See figure 4, C_L = 50 pF 7/	9,10,11	All	0	20	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol/ altern. symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit Min	Limit Max	Unit
Disable time, random output from $\overline{TRG}$ high 8/	$t_{dis(G)}$ t_{OEZ}	See figure 4, C_L = 50 pF 7/	9,10,11	All	0	20	ns
Disable time, random output from $\overline{WE}$ low 8/	$t_{dis(WL)}$ t_{WEZ}	See figure 4, C_L = 50 pF 7/	9,10,11	All	0	25	ns
Disable time, serial output from $\overline{SE}$ high 8/	$t_{dis(SE)}$ t_{SEZ}	See figure 4 C_L = 30 pF 7/	9,10,11	01	0	20	ns
				02	0	15	
				03	0	18	
Cycle time, read	$t_{c(RD)}$ t_{RC}	Timing measurements are referenced to V_{IL} max and V_{IH} min. See figure 4	9,10,11	01	150		ns
				02	130		
				03	140		
Cycle time, write	$t_{c(W)}$ t_{WC}		9,10,11	01	150		ns
				02	130		
				03	140		
Cycle time, read-modify-write	$t_{c(rdW)}$ t_{RMW}		9,10,11	01	200		ns
				02	175		
				03	188		
Cycle time, page-mode read, write	$t_{c(P)}$ t_{PC}		9,10,11	01	50		ns
				02	45		
				03	48		
Cycle time, page-mode read-modify-write	$t_{c(RDWP)}$ t_{PRMW}		9,10,11	01	90		ns
				02	85		
				03	88		
Cycle time, transfer read	$t_{c(TRD)}$ t_{RC}		9,10,11	01	150		ns
				02	130		
				03	140		
Cycle time, serial clock 9/	$t_{c(SC)}$ t_{SCC}		9,10,11	01	30		ns
				02	22		
				03	24		
Pulse duration, $\overline{CAS}$ high	$t_{w(CH)}$ t_{CPN}		9,10,11	All	10		ns
Pulse duration, $\overline{CAS}$ low 10/	$t_{w(CL)}$ t_{CAS}		9,10,11	All	20		ns
						10	µs
Pulse duration, $\overline{RAS}$ high	$t_{w(RH)}$ t_{RP}		9,10,11	01	60		ns
				02	50		
				03	55		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol/ altern. symbol	Conditions -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Pulse duration, $\overline{RAS}$ low 11/	$t_{w(RL)}$ t_{RAS}	Timing measurements are referenced to V_{IL} max and V_{IH} min. See figure 4	9,10,11	01	80		ns
				02	70		
				03	75		
				All		10	µs
Pulse duration, $\overline{WE}$ low	$t_{w(WL)}$ t_{WP}		9,10,11	01	15		ns
				02	10		
				03	13		
Pulse duration, $\overline{TRG}$ low	$t_{w(TRG)}$		9,10,11	All	20		ns
Pulse duration, SC high	$t_{w(SCH)}$ t_{SC}		9,10,11	01	10		ns
				02	8		
				03	9		
Pulse duration, SC low	$t_{w(SCL)}$ t_{SCP}		9,10,11	01	10		ns
				02	8		
				03	9		
Pulse duration, $\overline{TRG}$ high	$t_{w(GH)}$ t_{TP}		9,10,11	All	20		ns
Pulse duration, $\overline{RAS}$ low (page mode)	$t_{w(RL)P}$ t_{RASP}		9,10,11	01	80		ns
				02	70		
				03	75		
				All		100	µs
Setup time, column address before $\overline{CAS}$ low	$t_{su(CA)}$ t_{ASC}		9,10,11	All	0		ns
Setup time, DSF before $\overline{CAS}$ low	$t_{su(SFC)}$ t_{FSC}		9,10,11	All	0		ns
Setup time, row address before $\overline{RAS}$ low	$t_{su(RA)}$ t_{ASR}		9,10,11	All	0		ns
Setup time, $\overline{WE}$ before $\overline{RAS}$ low	$t_{su(WMR)}$ t_{WSR}		9,10,11	All	0		ns
Setup time, DQ before $\overline{RAS}$ low	$t_{su(DQR)}$ t_{MS}		9,10,11	All	0		ns
Setup time, $\overline{TRG}$ high before $\overline{RAS}$ low	$t_{su(TRG)}$ t_{THS}		9,10,11	All	0		ns
Setup time, DSF low before $\overline{RAS}$ low	$t_{su(SFR)}$ t_{FSR}		9,10,11	All	0		ns
Setup time, data valid before $\overline{CAS}$ low	$t_{su(DCL)}$ t_{DSC}		9,10,11	All	0		ns
Setup time, data valid before $\overline{WE}$ low	$t_{su(DWL)}$ t_{DSW}		9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol/ altern. symbol	Conditions -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limit Min	Limit Max	Unit
Setup time, read command, $\overline{WE}$ high before $\overline{CAS}$ low	$t_{su(rd)}$ t_{RCS}	Timing measurements are referenced to V_{IL} max and V_{IH} min. See figure 4	9,10,11	All	0		ns
Setup time, early write command, $\overline{WE}$ low before $\overline{CAS}$ low	$t_{su(WCL)}$ t_{WCS}		9,10,11	All	0		ns
Setup time, $\overline{WE}$ low before $\overline{CAS}$ high, write	$t_{su(WCH)}$ t_{CWL}		9,10,11	01	20		ns
				02	15		
				03	18		
Setup time, $\overline{WE}$ low before $\overline{RAS}$ high, write	$t_{su(WRH)}$ t_{RWL}		9,10,11	All	20		ns
Hold time, column address after $\overline{CAS}$ low	$t_{h(CLCA)}$ t_{CAH}		9,10,11	01	15		ns
				02	10		
				03	13		
Hold time, DSF after $\overline{CAS}$ low	$t_{h(SFC)}$ t_{CFH}		9,10,11	All	15		ns
Hold time, row address after $\overline{RAS}$ low	$t_{h(RA)}$ t_{RAH}		9,10,11	All	10		ns
Hold time, $\overline{TRG}$ after $\overline{RAS}$ low	$t_{h(TRG)}$ t_{THH}		9,10,11	All	15		ns
Hold time, write mask after $\overline{RAS}$ low	$t_{h(RWM)}$ t_{RWH}		9,10,11	All	15		ns
Hold time, DQ after $\overline{RAS}$ low (write-mask operation)	$t_{h(RDQ)}$ t_{MH}		9,10,11	All	15		ns
Hold time, DSF after $\overline{RAS}$ low	$t_{h(SFR)}$ t_{RFH}		9,10,11	All	10		ns
Hold time, column address valid after $\overline{RAS}$ low 12/	$t_{h(RLCA)}$ t_{AR}		9,10,11	01	35		ns
				02	30		
				03	33		
Hold time, data valid after $\overline{CAS}$ low	$t_{h(CLD)}$ t_{DH}		9,10,11	All	15		ns
Hold time, data valid after $\overline{RAS}$ low 12/	$t_{h(RLD)}$ t_{DHR}		9,10,11	All	35		ns
Hold time, data valid after $\overline{WE}$ low	$t_{h(WLD)}$ t_{DH}		9,10,11	All	15		ns
Hold time, read, $\overline{WE}$ high after $\overline{CAS}$ high 13/	$t_{h(CHrd)}$ t_{RCH}		9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol/ altern. symbol	Conditions -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Hold time, read, $\overline{WE}$ high after $\overline{RAS}$ high 13/	$t_{h(RHrd)}$ t_{RRH}	Timing measurements are referenced to V_{IL} max and V_{IH} min. See figure 4	9,10,11	All	0		ns
Hold time, write, $\overline{WE}$ low after $\overline{CAS}$ low	$t_{h(CLW)}$ t_{WCH}		9,10,11	All	15		ns
Hold time, write, $\overline{WE}$ low after $\overline{RAS}$ low 12/	$t_{h(RLW)}$ t_{WCR}		9,10,11	All	35		ns
Hold time, $\overline{TRG}$ high after $\overline{WE}$ low 14/	$t_{h(WLG)}$ t_{OEH}		9,10,11	All	10		ns
Hold time, SQ valid after SC high	$t_{h(SHSQ)}$ t_{SOH}		9,10,11	All	2		ns
Hold time, DSF after $\overline{RAS}$ low	$t_{h(RSF)}$ t_{FHR}		9,10,11	All	35		ns
Hold time, output valid after $\overline{CAS}$ low	$t_{h(CLQ)}$ t_{DHC}		9,10,11	All	0		ns
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	$t_{d(RLCH)}$ t_{CSH}		9,10,11	01	80		ns
				02	70		
				03	75		
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high 15/	$t_{d(RLCH)}$ t_{CHR}		9,10,11	01	15		ns
				02	10		
				03	13		
Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	$t_{d(CHRL)}$ t_{CRP}		9,10,11	All	0		ns
Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	$t_{d(CLRH)}$ t_{RSH}		9,10,11	All	20		ns
Delay time, $\overline{CAS}$ low to $\overline{WE}$ low 16/ 17/	$t_{d(CLWL)}$ t_{CWD}		9,10,11	01	50		ns
				02	45		
				03	48		
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low 18/	$t_{d(RLCL)}$ t_{RCD}		9,10,11	01	20	60	ns
				02,03	20	50	
Delay time, column address valid to $\overline{RAS}$ high	$t_{d(CARH)}$ t_{RAL}		9,10,11	01	40		ns
				02	35		
				03	38		
Delay time, column address valid to $\overline{CAS}$ high	$t_{d(CACH)}$ t_{CAL}		9,10,11	01	40		ns
				02	35		
				03	38		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol/ altern. symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5 V \le V_{CC} \le 5.5 V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{WE}}$ low 16/	$t_{d(RLWL)}$ t_{RWD}	Timing measurements are referenced to V_{IL} max and V_{IH} min. See figure 4	9,10,11	01	105		ns
				02	95		
				03	100		
Delay time, column address valid to $\overline{\text{WE}}$ low 16/	$t_{d(CAWL)}$ t_{AWD}		9,10,11	01	65		ns
				02	60		
				03	63		
Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ low 15/	$t_{d(CLRL)}$ t_{CSR}		9,10,11	All	0		ns
Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low 15/	$t_{d(RHCL)}$ t_{RPC}		9,10,11	All	0		ns
Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{TRG}}$ high for DRAM read cycles	$t_{d(CLGH)}$		9,10,11	All	20		ns
Delay time, $\overline{\text{TRG}}$ high before data applied at DQ	$t_{d(GHD)}$ t_{OED}		9,10,11	All	15		ns
Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{TRG}}$ high 19/	$t_{d(RLTH)}$ t_{RTH}		9,10,11	01	60		ns
				02	55		
				03	58		
Delay time, $\overline{\text{RAS}}$ low to first SC high after $\overline{\text{TRG}}$ high 20/	$t_{d(RLSH)}$ t_{RSD}		9,10,11	01	80		ns
				02	70		
				03	75		
Delay time, $\overline{\text{RAS}}$ low to column address valid	$t_{d(RLCA)}$ t_{RAD}		9,10,11	01	15	40	ns
				02,03	15	35	
Delay time, $\overline{\text{TRG}}$ low to $\overline{\text{RAS}}$ high	$t_{d(GLRH)}$ t_{ROH}		9,10,11	All	20		ns
Delay time, $\overline{\text{CAS}}$ low to first SC high after $\overline{\text{TRG}}$ high 20/	$t_{d(CLSH)}$ t_{CSD}		9,10,11	01	25		ns
				02	20		
				03	23		
Delay time, SC high to $\overline{\text{TRG}}$ high 19/ 20/	$t_{d(SCTR)}$ t_{TSL}		9,10,11	All	5		ns
Delay time, $\overline{\text{TRG}}$ high to $\overline{\text{RAS}}$ high 19/	$t_{d(THRH)}$ t_{TRD}		9,10,11	All	-10		ns
Delay time, $\overline{\text{TRG}}$ high to $\overline{\text{RAS}}$ low 21/	$t_{d(THRL)}$ t_{TRP}		9,10,11	01	60		ns
				02	50		
				03	55		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol/ altern. symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit Min	Limit Max	Unit
Delay time, $\overline{TRG}$ high to SC high 19/	$t_{d(THSC)}$ t_{TSD}	Timing measurements are referenced to V_{IL} max and V_{IH} min. See figure 4	9,10,11	01	20		ns
				02	15		
				03	18		
Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split-register transfer read cycles	$t_{d(RHMS)}$		9,10,11	All	20		ns
Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high in real-time transfer read cycles	$t_{d(CLTH)}$ t_{CTH}		9,10,11	All	15		ns
Delay time, column address to first SC in early-load transfer read cycles	$t_{d(CASH)}$ t_{ASD}		9,10,11	01	30		ns
				02	25		
				03	28		
Delay time, column address to $\overline{TRG}$ high in real-time transfer read cycles	$t_{d(CAGH)}$ t_{ATH}		9,10,11	All	20		ns
Delay time, data to $\overline{CAS}$ low	$t_{d(DCL)}$ t_{DZC}		9,10,11	All	0		ns
Delay time, data to $\overline{TRG}$ low	$t_{d(DGL)}$ t_{DZO}		9,10,11	All	0		ns
Delay time, last (most significant) rising edge of SC to $\overline{RAS}$ low before boundary switch during split-register transfer read cycles	$t_{d(MSRL)}$		9,10,11	All	20		ns
Delay time, last (127 or 255) rising edge of SC to QSF switching at the boundary during split-register transfer read cycles 22/	$t_{d(SC\ QSF)}$ t_{SQD}		9,10,11	01		30	ns
				02		25	
				03		28	
Delay time, $\overline{CAS}$ low to QSF switching in transfer read cycles 22/	$t_{d(CLQSF)}$ t_{CQD}		9,10,11	01		35	ns
				02		30	
				03		33	
Delay time, $\overline{TRG}$ high to QSF switching in transfer read cycles 22/	$t_{d(GHQSF)}$ t_{CQD}		9,10,11	01		30	ns
				02		25	
				03		28	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol/ altern. symbol	Conditions -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limit Min	Limit Max	Unit
Delay time, $\overline{RAS}$ low to QSF switching in transfer read cycles 22/	$t_{d(RLQSF)}$ t_{RQD}		9,10,11	01		75	ns
				02		70	
				03		73	
Refresh time interval, memory	$t_{rf(MA)}$ t_{REF}		9,10,11	All		8	ms
Transition time	t_t t_T		9,10,11	All	3	50	ns

1/ For conditions shown as Min/Max, use the appropriate value specified in the timing requirements.

2/ $\overline{SE}$ is disabled for SQ output leakage tests.

3/ Measured with one address change while $\overline{RAS}$ = V_{IL}. $t_{c(rd)}$, $t_{c(W)}$, $t_{c(TRD)}$ = Min.

4/ Measured with output open.

5/ Measured with one address change while $\overline{CAS}$ = V_{IH}.

6/ V_{CC} = 5 V ±0.5 V, and the bias on pins under test is 0 V.

7/ Switching times for RAM port output are measured with a load equivalent to 1 TTL load and 50 pF. Data-out reference level: V_{OH} / V_{OL} = 2 V / 0.8 V. Switching times for SAM port output are measured with a load equivalent to 1 TTL load and 30 pF. Serial data-out reference level: V_{OH} / V_{OL} = 2 V / 0.8 V.

8/ $t_{dis(CH)}$, $t_{dis(RH)}$, $t_{dis(G)}$, $t_{dis(WL)}$ and $t_{dis(SE)}$ are specified when the output is no longer driven.

9/ Cycle time assumes t_t = 3 ns.

10/ In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the users's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].

11/ In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the users's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

12/ The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.

13/ Either $t_{h(RHrd)}$ or $t_{d(CHrd)}$ must be satisfied for a read cycle.

14/ Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.

15/ $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only.

16/ Read-modify-write operation only.

17/ $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.

18/ The maximum value is specified only to assure $\overline{RAS}$ access time.

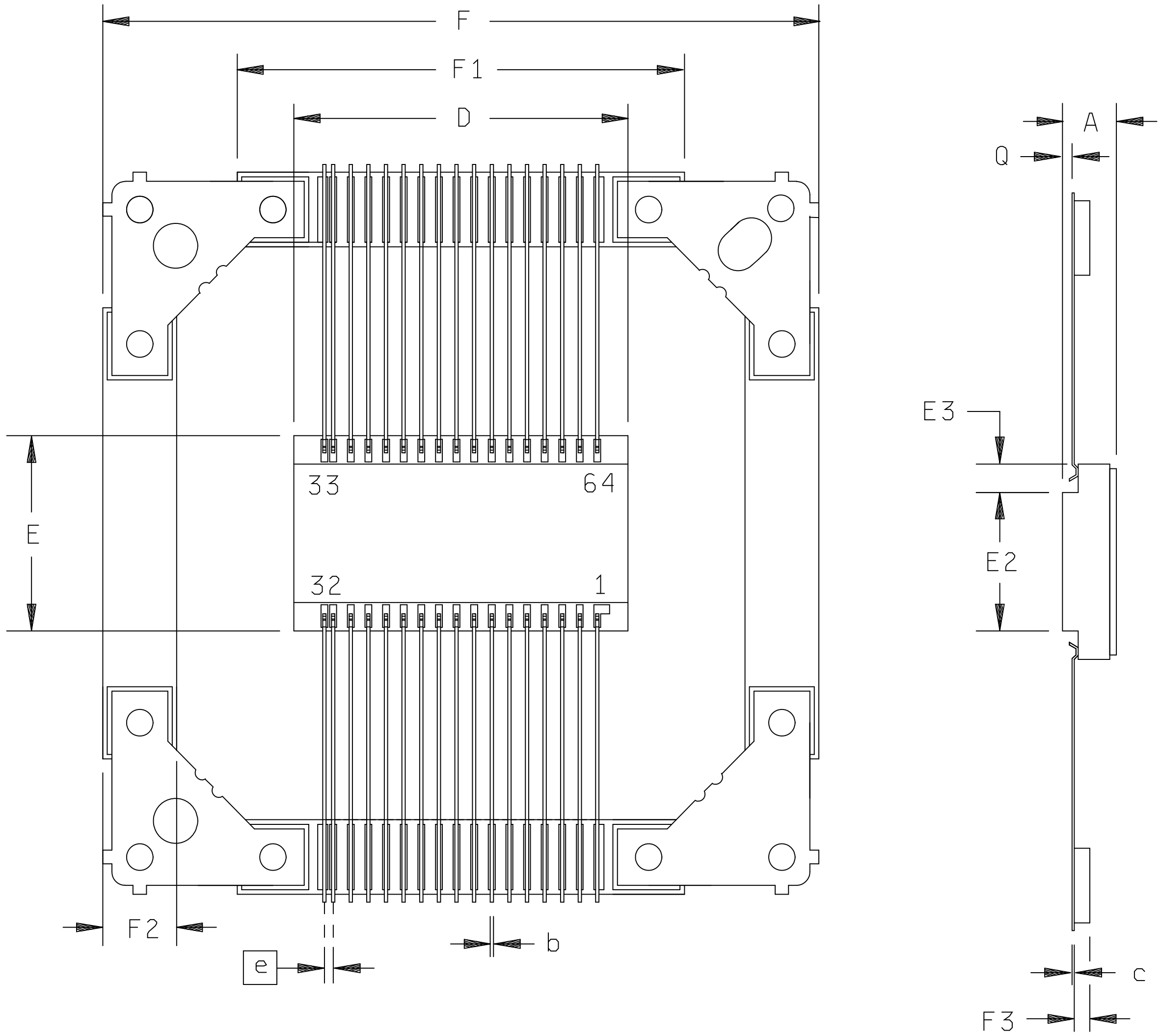
19/ Real-time load transfer read or late-load transfer read cycle only.

20/ Early-load transfer read cycle only.

21/ Full-register (read) transfer cycles only.

22/ Switching times for QSF output are measured with a load equivalent to 1 TTL load and 30 pF, and output reference level is V_{OH} / V_{OL} = 2 V / 0.8 V.

Case Y



Symbol	Millimeters	
	Min	Max
A	2.54	3.81
b	0.15	0.25
c	0.11	0.20
D	18.54	19.43
E	10.67	11.30
E2	7.49	8.13
E3	1.40	1.78
e	0.50 BSC	
F	40.13	41.14
F1	24.89	25.91
F2	3.68	4.70
F3	0.76	1.02
Q	0.66	---

FIGURE 1. Case outline.

Device types: All																	
Case outline: X (Bottom view)																	
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
J1	DQ_1	J2	SQ_3	J3	DQ_3	J4	DQ_4	J5	DQ_5	J6	DQ_6	J7	SQ_7	J8	$\overline{CASL}$	J9	A_8
H1	DQ_0	H2	SQ_2	H3	DQ_2	H4	SQ_4	H5	SQ_5	H6	SQ_6	H7	DQ_7	H8	$\overline{WE}$	H9	A_7
G1	SQ_0	G2	SQ_1	G3	V_{DD2}	G4	V_{SS2}			G6	V_{DD2}	G7	V_{SS2}	G8	$\overline{RAS}$	G9	A_6
F1	$\overline{TRG}$	F2	V_{SS1}	F3	V_{DD1}							F7	V_{DD1}	F8	V_{DD1}	F9	A_5
E1	SC	E2	V_{DD1}											E8	V_{SS1}	E9	A_4
D1	$\overline{SE}$	D2	V_{SS1}	D3	V_{DD1}							D7	V_{SS1}	D8	A_3	D9	A_2
C1	SQ_{15}	C2	V_{SS1}	C3	V_{DD2}	C4	V_{SS2}			C6	V_{DD2}	C7	V_{SS2}	C8	$\overline{CASU}$	C9	A_1
B1	DQ_{15}	B2	DQ_{14}	B3	DQ_{13}	B4	DQ_{12}	B5	DQ_{11}	B6	DQ_{10}	B7	SQ_8	B8	DSF	B9	A_0
A1	SQ_{14}	A2	SQ_{13}	A3	SQ_{12}	A4	SQ_{11}	A5	SQ_{10}	A6	SQ_9	A7	DQ_9	A8	DQ_8	A9	QSF

FIGURE 2. <u>Terminal connections</u>.

Device types	All	Device types	All
Case Outline	Y	Case Outline	Y
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	V_{CC}	33	V_{SS}
2	$\overline{TRG}$	34	A_3
3	V_{SS}	35	A_2
4	SQ_0	36	A_1
5	DQ_0	37	A_0
6	SQ_1	38	QSF
7	DQ_1	39	$\overline{CASU}$
8	V_{CC}	40	NC / GND
9	SQ_2	41	D_{SF}
10	DQ_2	42	V_{SS}
11	SQ_3	43	DQ_8
12	DQ_3	44	SQ_8
13	V_{SS}	45	DQ_9
14	SQ_4	46	SQ_9
15	DQ_4	47	V_{CC}
16	SQ_5	48	DQ_{10}
17	DQ_5	49	SQ_{10}
18	V_{CC}	50	DQ_{11}
19	SQ_6	51	SQ_{11}
20	DQ_6	52	V_{SS}
21	SQ_7	53	DQ_{12}
22	DQ_7	54	SQ_{12}
23	V_{SS}	55	DQ_{13}
24	$\overline{CASL}$	56	SQ_{13}
25	$\overline{WE}$	57	V_{CC}
26	$\overline{RAS}$	58	DQ_{14}
27	A_8	59	SQ_{14}
28	A_7	60	DQ_{15}
29	A_6	61	SQ_{15}
30	A_5	62	V_{SS}
31	A_4	63	$\overline{SE}$
32	V_{CC}	64	SC

FIGURE 2. Terminal connections - continued.

FUNCTION	$\overline{RAS}$ FALL				$\overline{CAS}$ FALL	ADDRESS		DQ0-DQ15 1/		MNE CODE
	$\overline{CASx}$ 2/	TRG	$\overline{WE}$	DSF	DSF	$\overline{RAS}$	$\overline{CASx}$ 3/	$\overline{RAS}$	$\overline{CASL}$ $\overline{CASU}$ $\overline{WE}$	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	--
$\overline{CAS}$ -before- $\overline{RAS}$ -refresh (no reset) and stop point set 4/	L	X	L	H	X	Stop point 5/	X	X	X	CBRS
$\overline{CAS}$ -before- $\overline{RAS}$ -refresh (option reset) 6/	L	X	H	L	X	X	X	X	X	CBR
$\overline{CAS}$ -before- $\overline{RAS}$ -refresh (no reset) 7/	L	X	H	H	X	X	X	X	X	CBRN
Full-register transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2-A8	Write Mask	Col Mask	BWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2-A8	X	Col Mask	BWM
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2-A8	X	Col Mask	BW
Load write-mask register 8/	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

X = Don't care Col Mask = H: Write to address/column enabled Write Mask = H: Write to I/O enabled

1/ DQ0-DQ15 are latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later.

2/ Logic L is selected when either or both $\overline{CASL}$ and $\overline{CASU}$ are low.

3/ The column address and block address are latched on the first falling edge of $\overline{CASx}$.

4/ CBRS cycle should be performed immediately after the power-up initialization cycle.

5/ A0-A3, A8: don't care; A4-A7: stop-point code.

6/ $\overline{CAS}$ -before- $\overline{RAS}$ -refresh (option reset) mode will end persistent write-per-bit mode and stop-point mode.

7/ $\overline{CAS}$ -before- $\overline{RAS}$ -refresh (no reset) mode will not end persistent write-per-bit mode or stop-point mode.

8/ Load-write-mask-register cycle will set the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the $\overline{CAS}$ -before- $\overline{RAS}$ -refresh (option reset) cycle.

FIGURE 3. Truth tables.

READ-CYCLE TIMING WITH $\overline{CASx}$-CONTROLLED OUTPUT

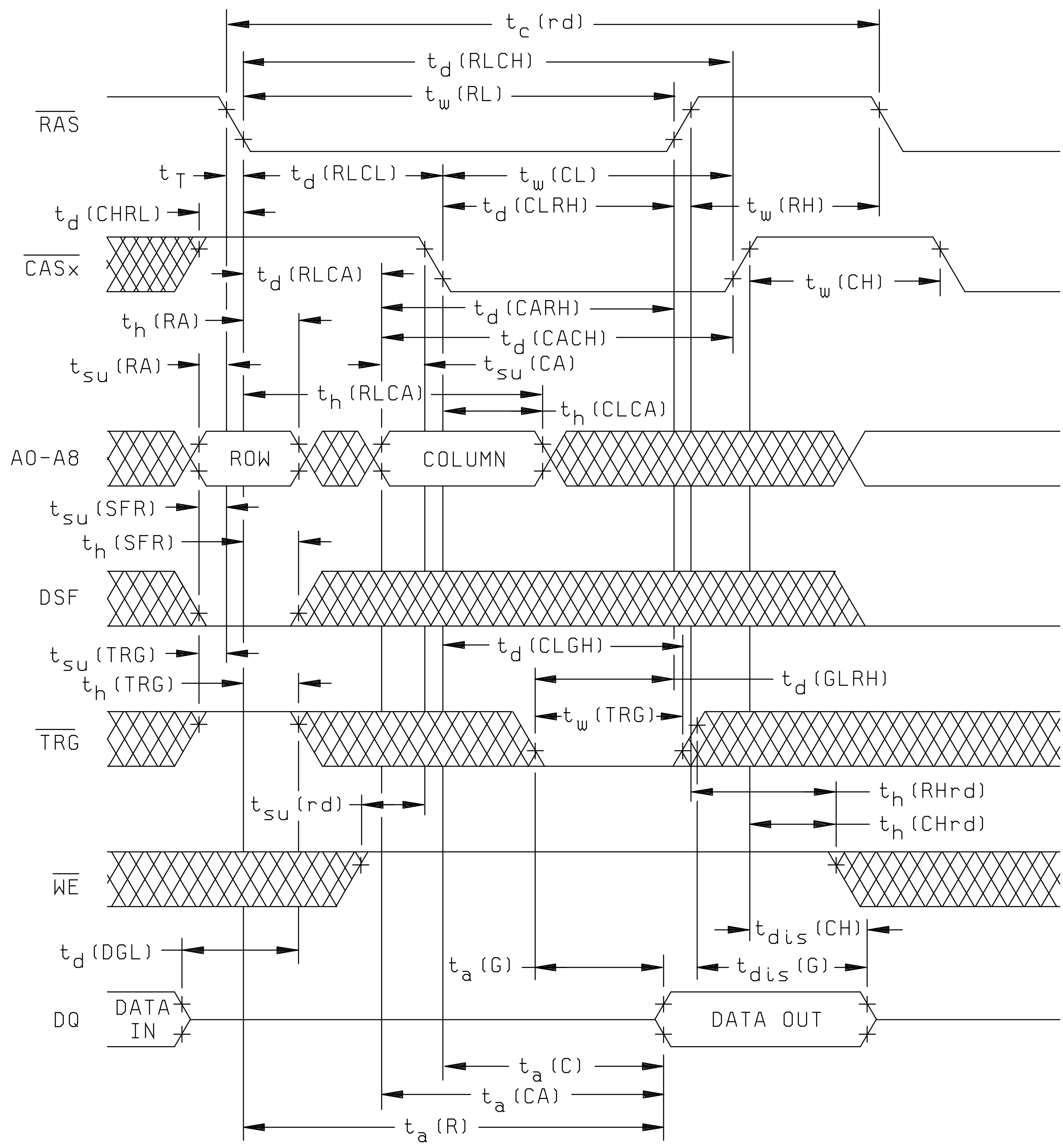


FIGURE 4. Timing waveform.

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READ-CYCLE TIMING WITH $\overline{RAS}$-CONTROLLED OUTPUT

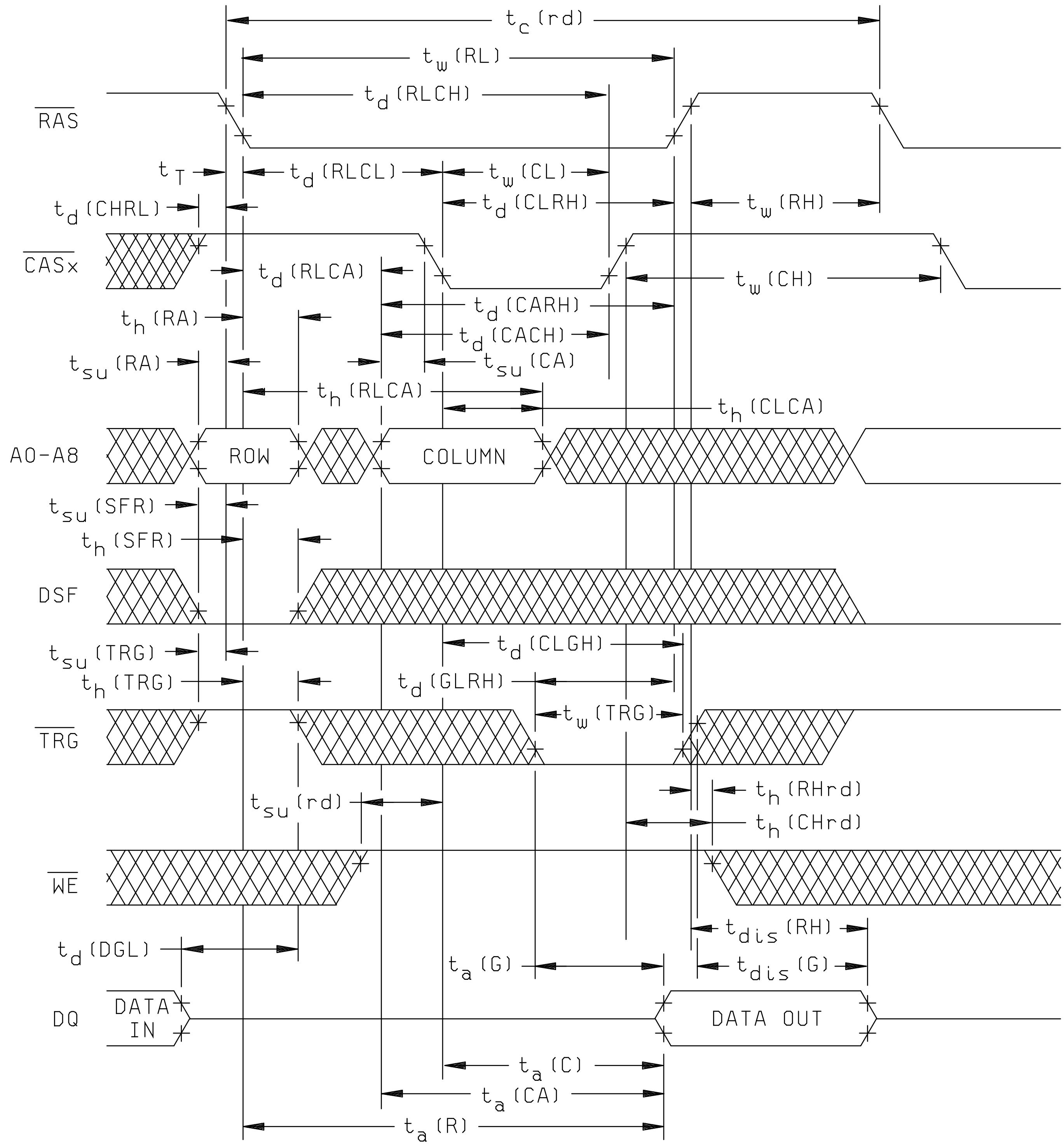
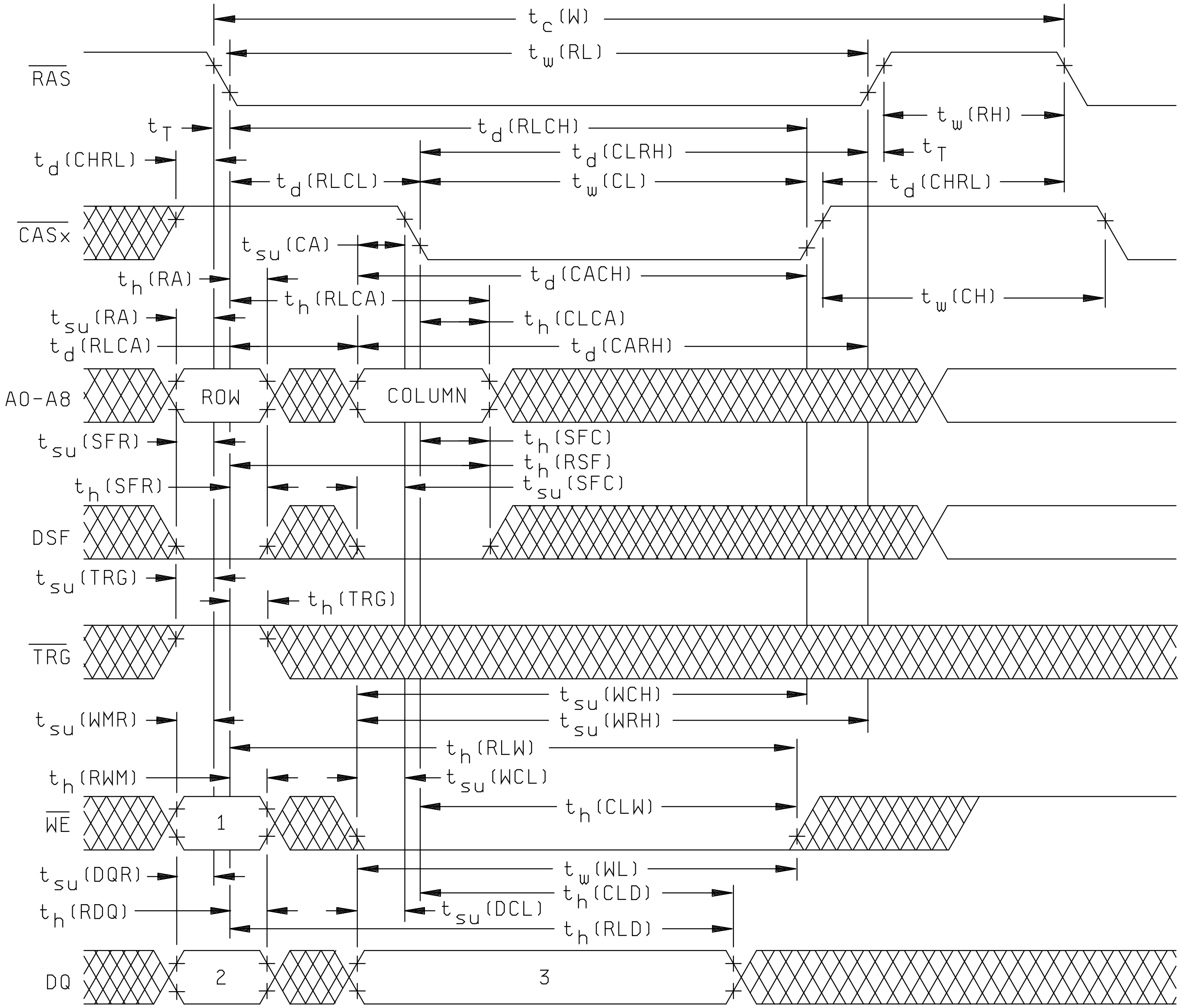


FIGURE 4. Timing waveform - continued.

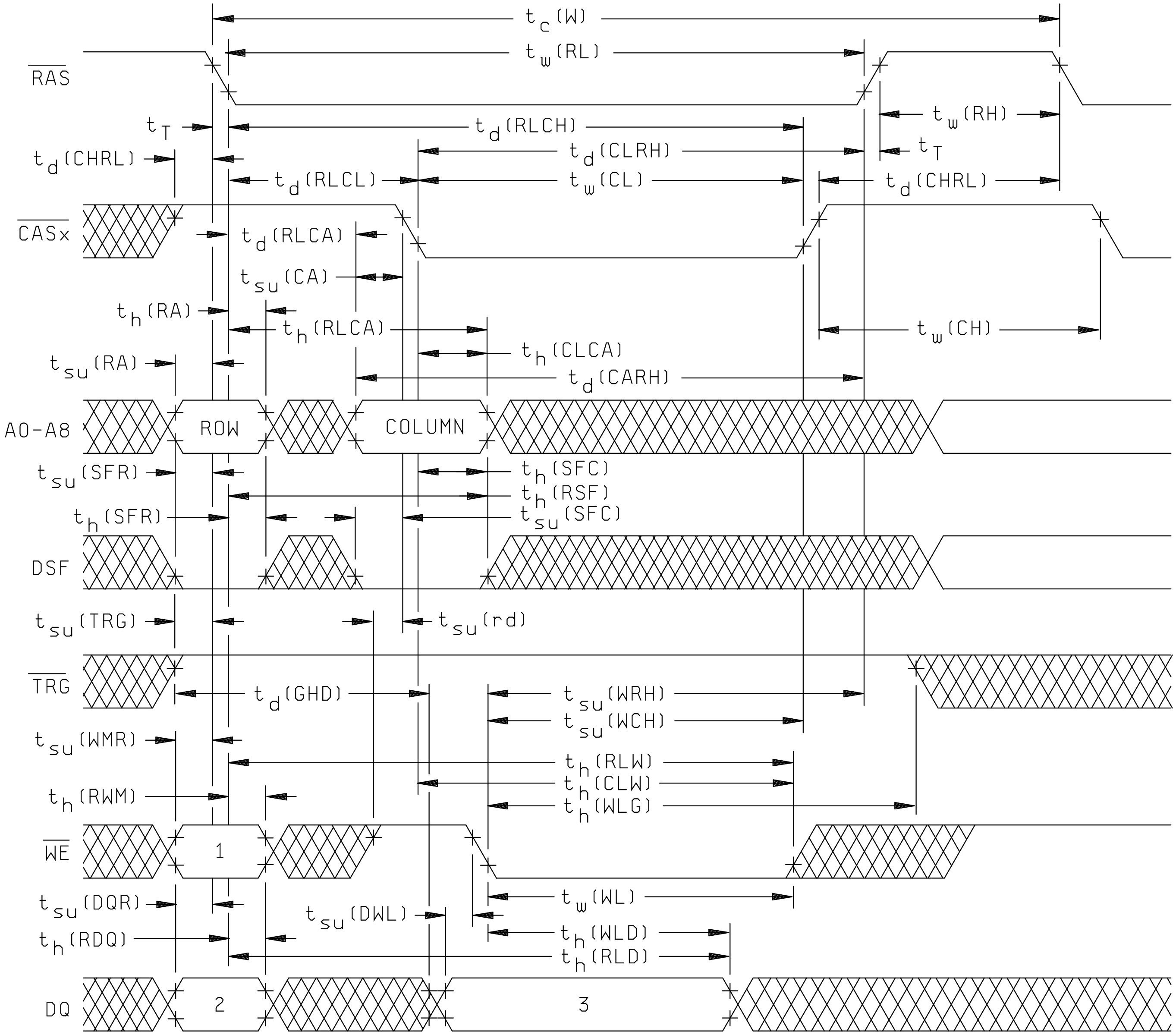
EARLY-WRITE-CYCLE TIMING



Cycle	State		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent w/B	L	Write mask	Valid data
Write operation with persistent w/B	L	Don't care	Valid data

FIGURE 4. Timing waveforms - continued.

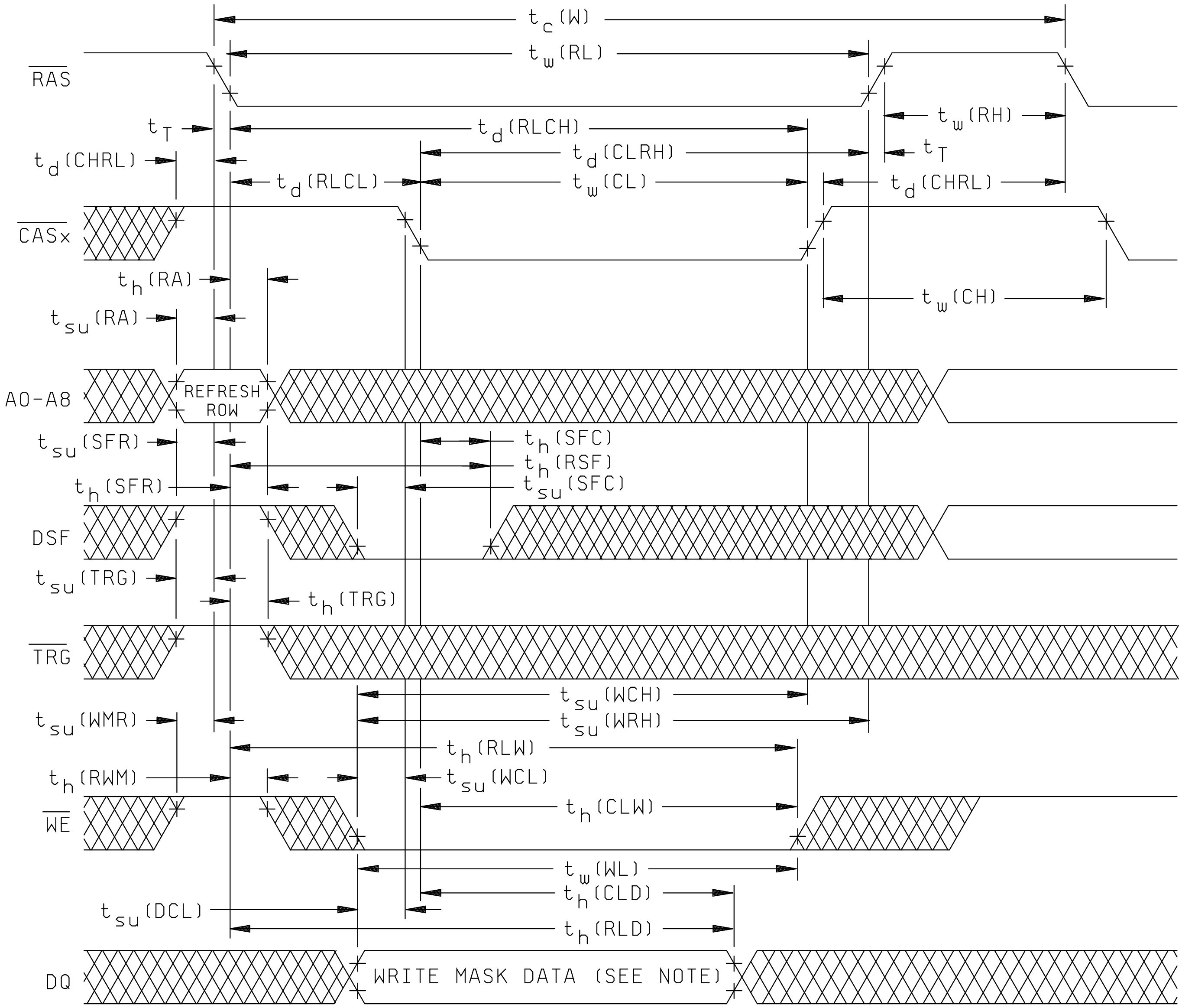
LATE-WRITE-CYCLE TIMING (OUTPUT-ENABLE-CONTROLLED WRITE)



Cycle	State		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent w/B	L	Write mask	Valid data
Write operation with persistent w/B	L	Don't care	Valid data

FIGURE 4. Timing waveforms - continued.

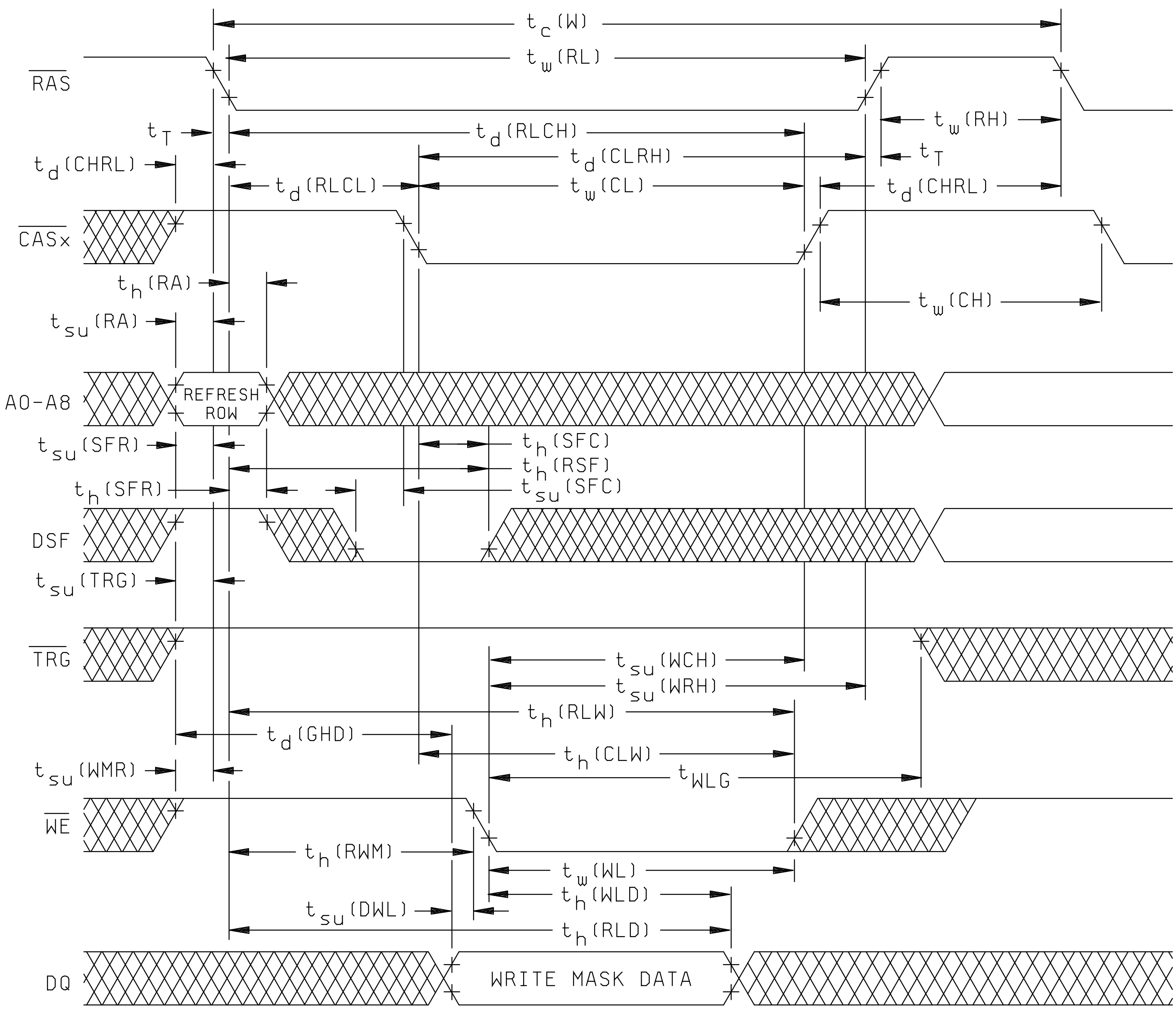
LOAD-WRITE-MASK-REGISTER-CYCLE TIMING (EARLY-WRITE LOAD)



NOTE: Load-write-mask-register cycle will put the device into the persistent write-per-bit mode.

FIGURE 4. Timing waveforms - continued.

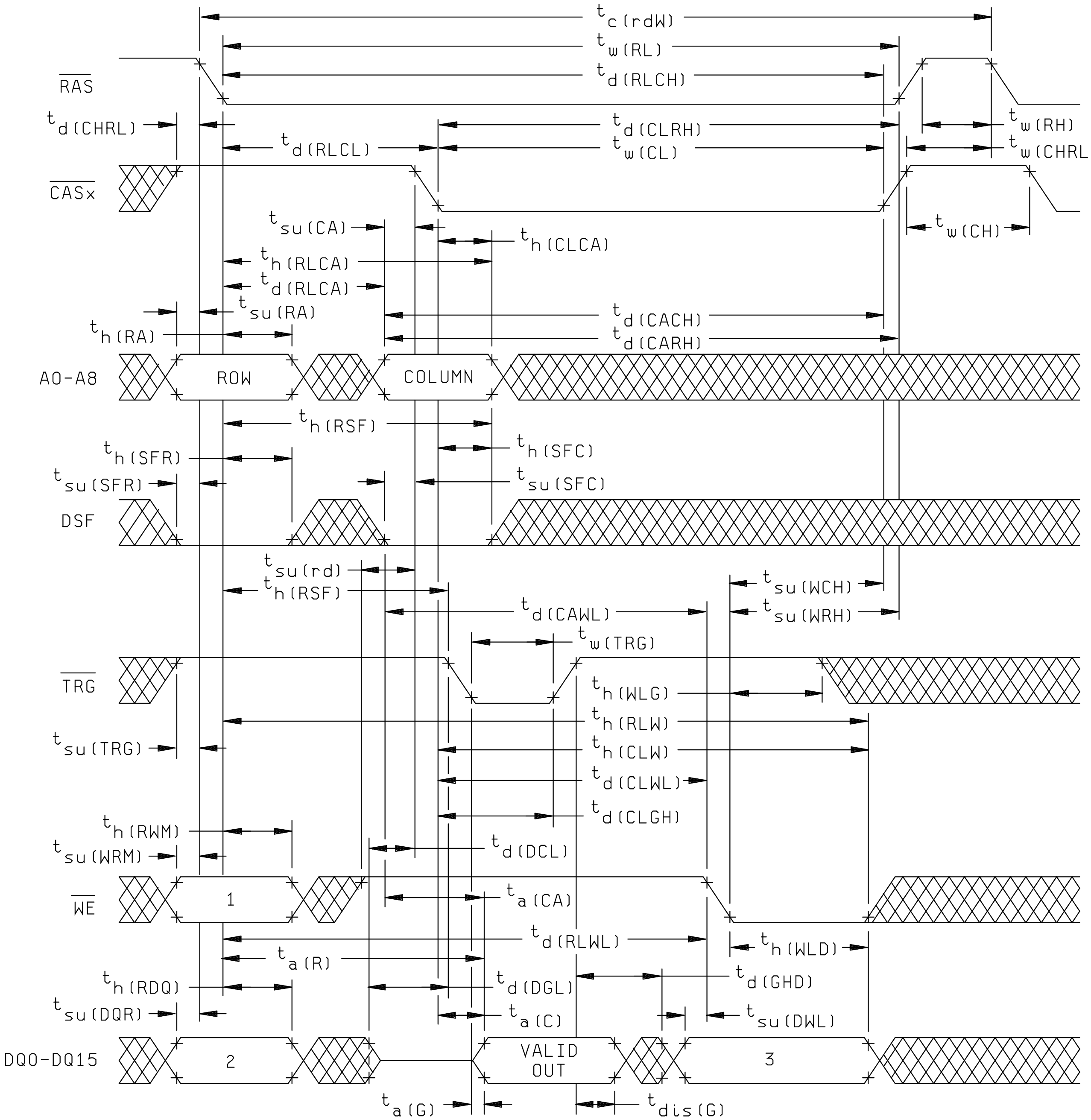
LOAD-WRITE-MASK-REGISTER-CYCLE TIMING (LATE-WRITE LOAD)



NOTE: Load-write-mask-register cycle will put the device into the persistent write-per-bit mode.

FIGURE 4. Timing waveforms - continued.

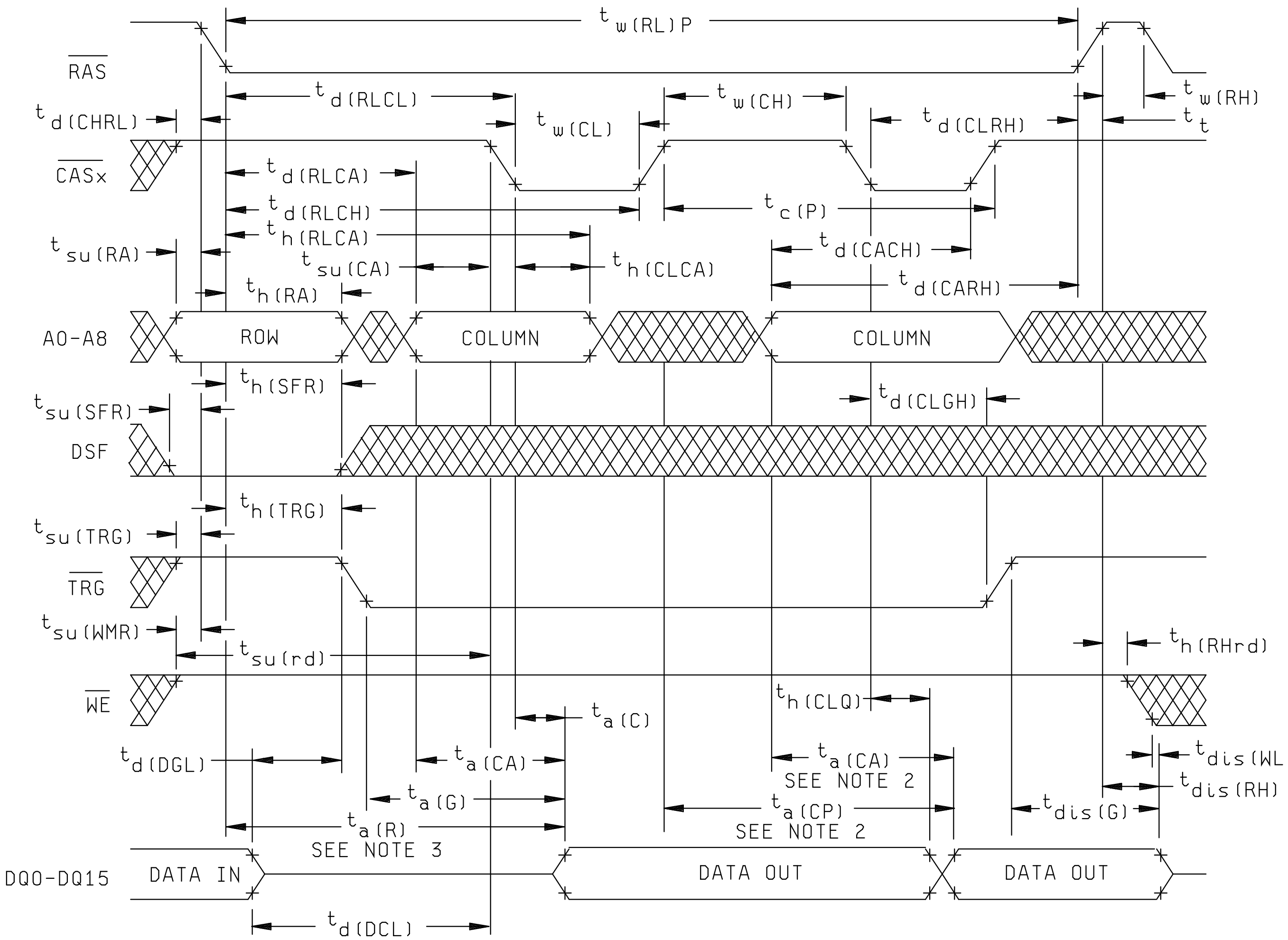
READ-WRITE/READ-MODIFY-WRITE-CYCLE TIMING



Cycle	State		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent w/B	L	Write mask	Valid data
Write operation with persistent w/B	L	Don't care	Valid data

FIGURE 4. Timing waveforms - continued.

ENHANCED PAGE-MODE READ CYCLE TIMING
SEE NOTE 1

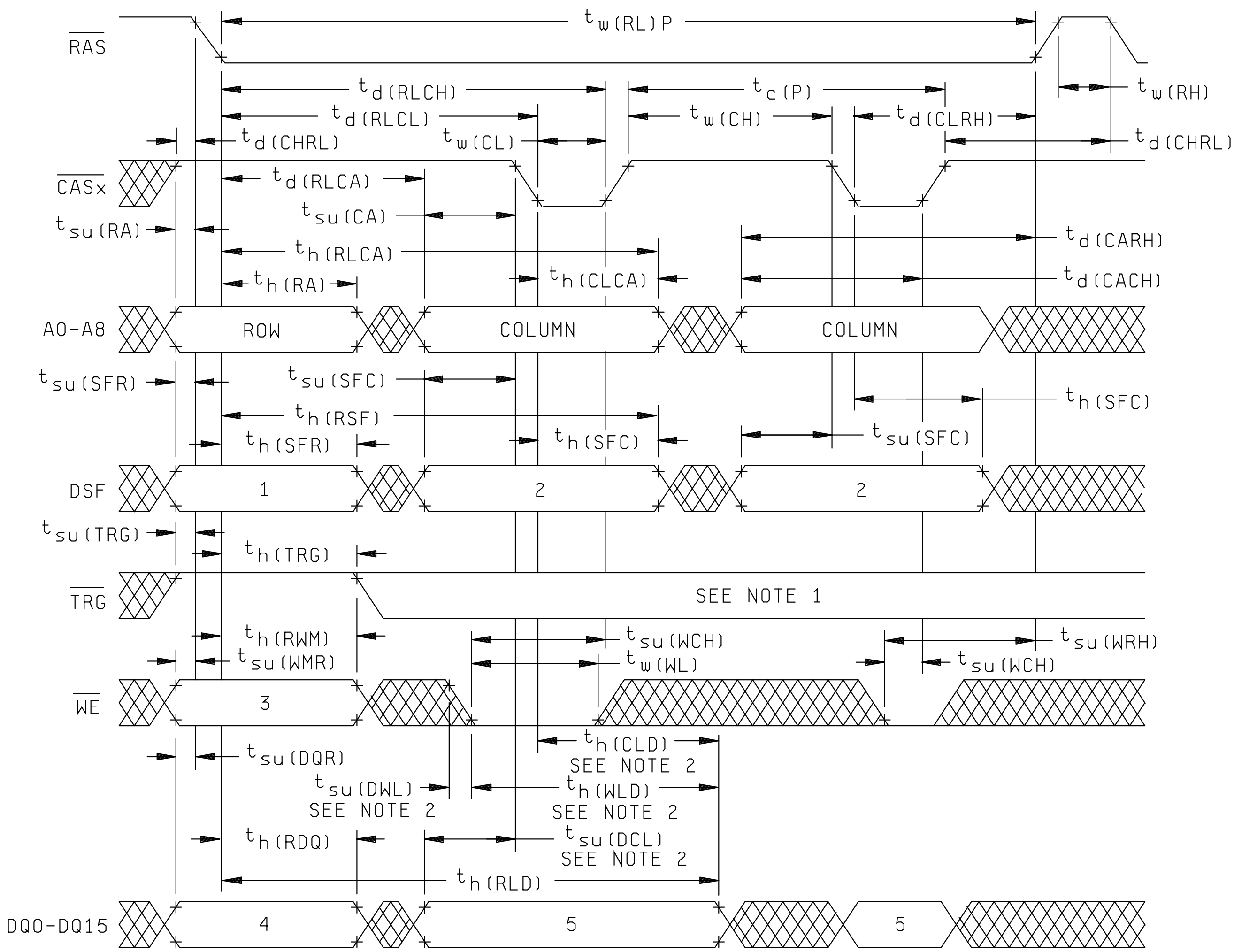


NOTES:

1. A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to select the desired write mode (normal, block write, etc.).
2. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
3. Output can go from the high-impedance state to an invalid data state prior to the specified access time.

FIGURE 4. Timing waveforms - continued.

ENHANCED-PAGE-MODE WRITE-CYCLE TIMING



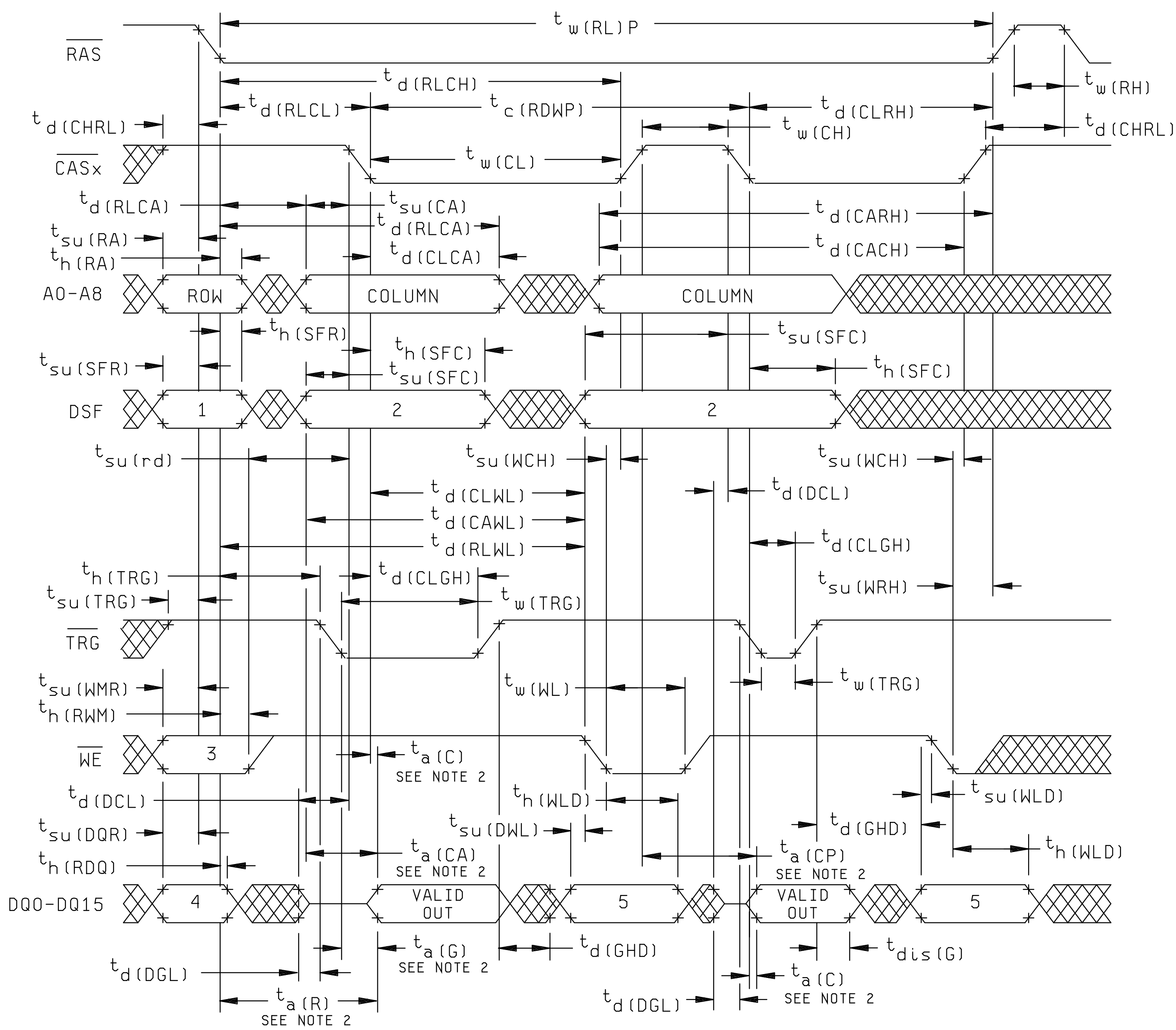
Cycle	State				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent w/B	L	L	L	Write mask	Valid data
Write operation with persistent w/B	L	L	L	Don't care	Valid data
Load write mask on first falling edge of CASx or or the falling edge of WE , whichever occurs later	H	L	H	Don't care	Write mask

NOTES:

1. A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. To assure page-mode cycle time, TRG must remain high throughout the entire page-mode operation if the late write feature is used. If the early write-cycle timing is used, the state of TRG is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of RAS .
2. Referenced to the first falling edge of CAS or the falling edge or WE , whichever occurs later.

FIGURE 4. Timing waveforms - continued.

ENHANCED-PAGE-MODE READ-MODIFY-WRITE-CYCLE TIMING(SEE NOTE 1)



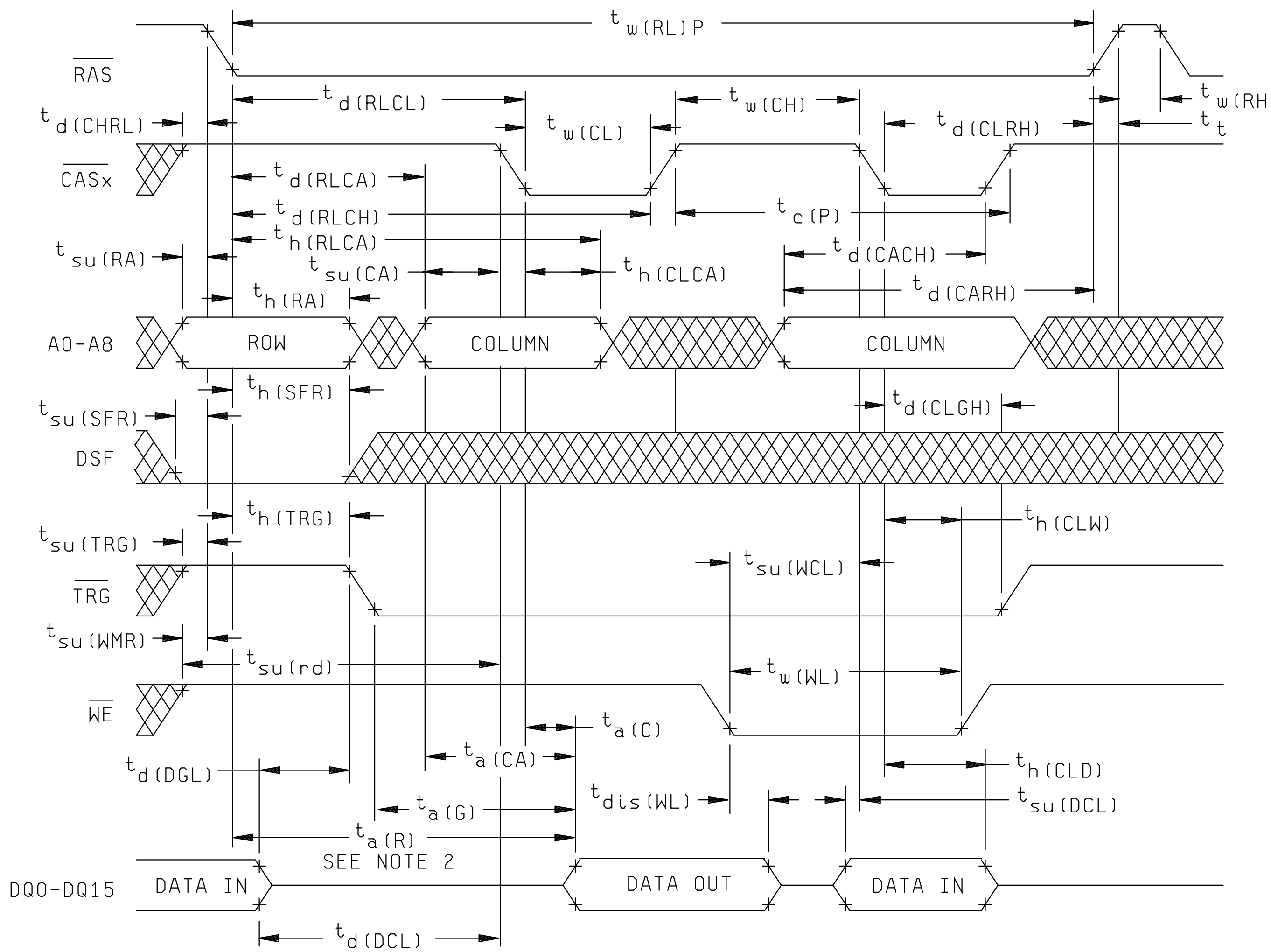
NOTES:

Cycle	State				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent w/B	L	L	L	Write mask	Valid data
Write operation with persistent w/B	L	L	L	Don't care	Valid data
Load write mask on first falling edge of CASx or or the falling edge of WE , whichever occurs later	H	L	H	Don't care	Write mask

1. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.
2. Output can go from the high-impedance state to an invalid data state prior to the specified access time.

FIGURE 4. Timing waveforms - continued.

ENHANCED-PAGE-MODE READ/WRITE-CYCLE TIMING (SEE NOTE 1)



NOTES:
1. A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specification are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to select the desired write mode (normal, block write, etc.).
2. Output can go from the high-impedance state to an invalid data state prior to the specified access time.

FIGURE 4. Timing waveforms - continued.

LOAD-COLOR-REGISTER-CYCLE TIMING(EARLY-WRITE LOAD)

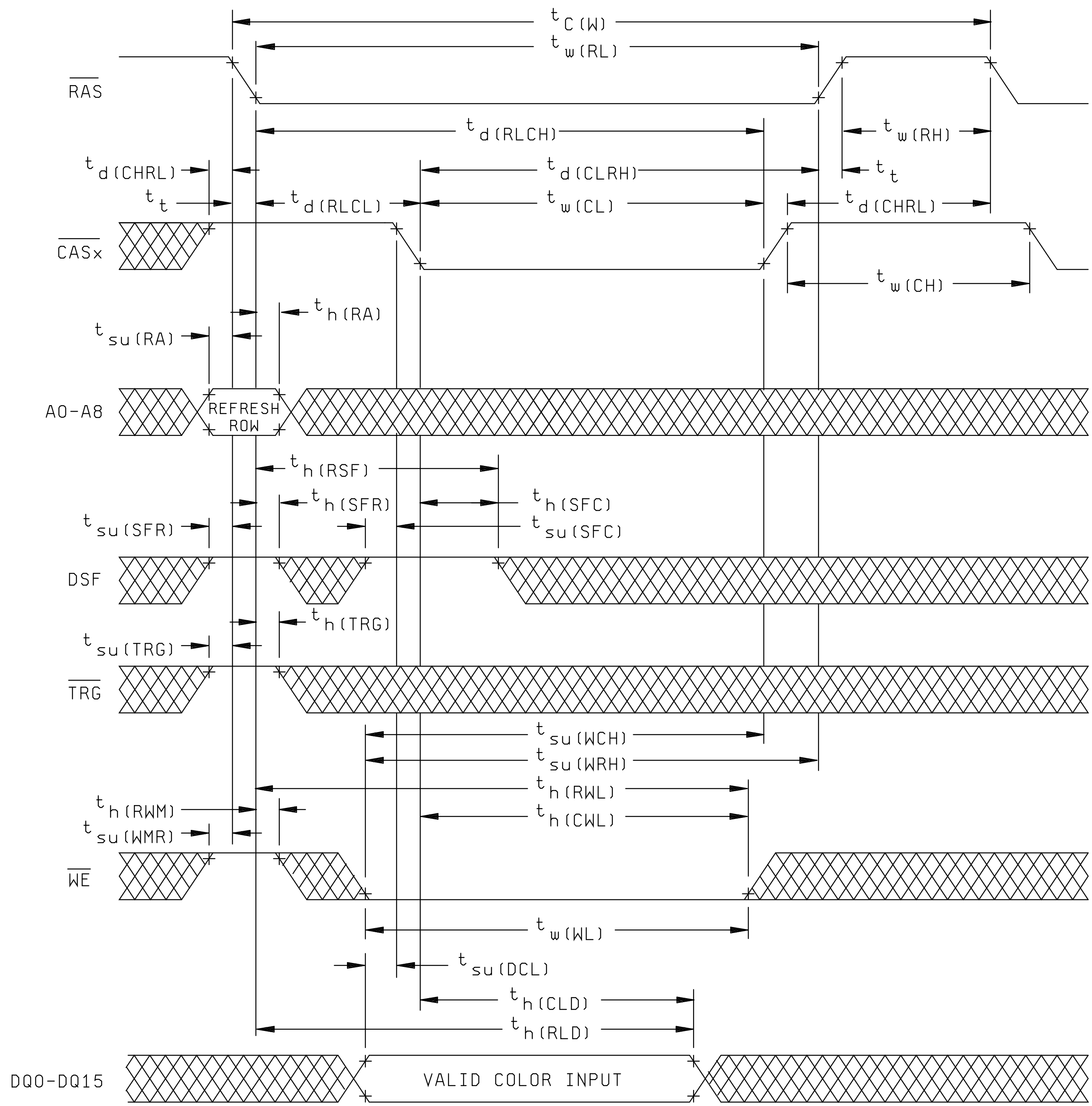


FIGURE 4. Timing waveforms - continued.

LOAD-COLOR-REGISTER-CYCLE TIMING(LATE-WRITE LOAD)

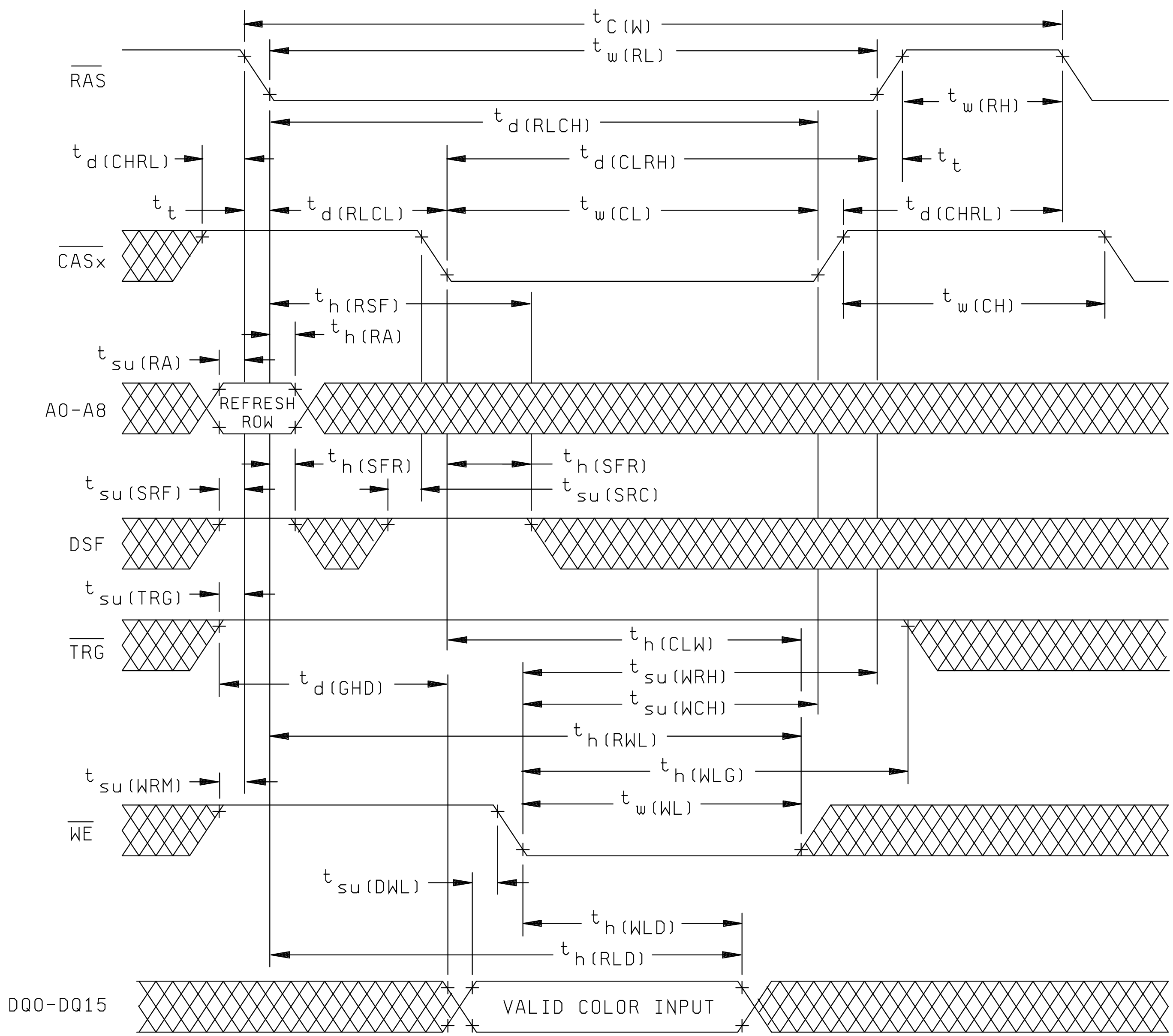
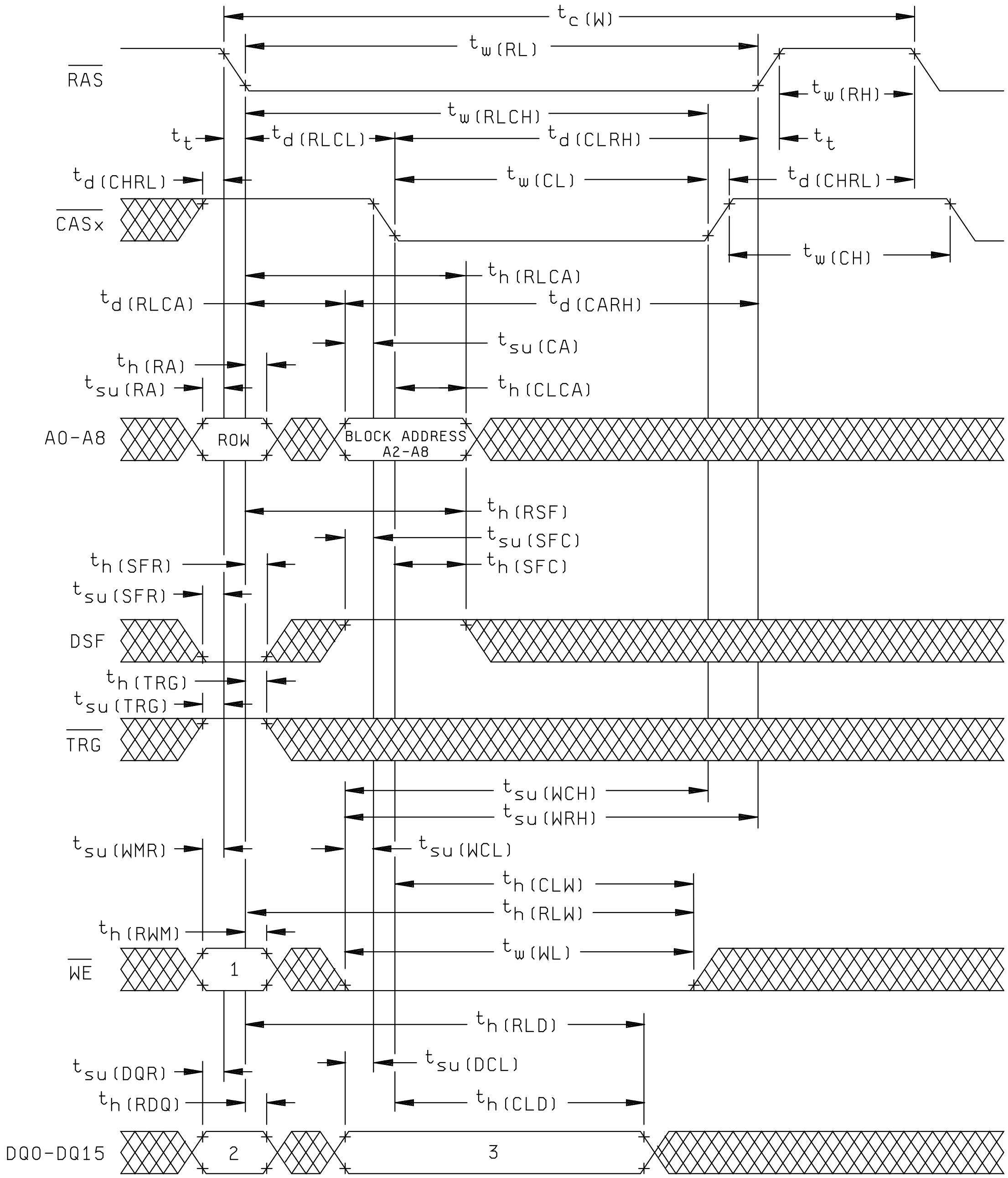


FIGURE 4. Timing waveforms - continued.

BLOCK-WRITE-CYCLE TIMING (EARLY-WRITE)

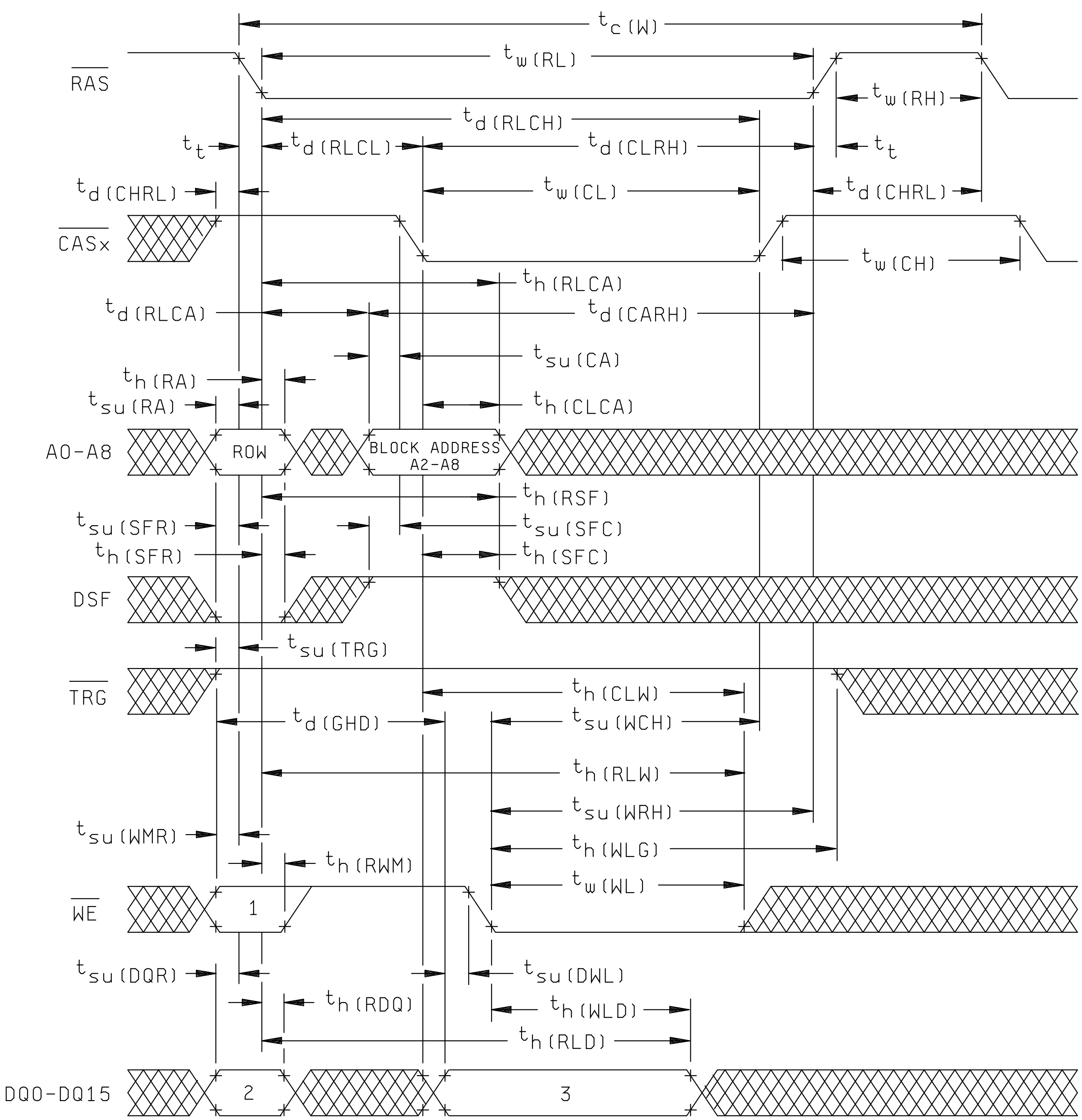


Cycle	State		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent w/B	L	Write mask	Column mask
Block-write operation with persistent w/B	L	Don't care	Column mask

For write-mask data, 0 = I/O write disable, 1 = I/O write enable.
For column-mask data (DQI to DQI + 3; I = 0, 4, 8, 12), 0 = column write disable, 1 = column write enable.

FIGURE 4. Timing waveforms - continued.

BLOCK-WRITE-CYCLE TIMIMG (LATE-WRITE)

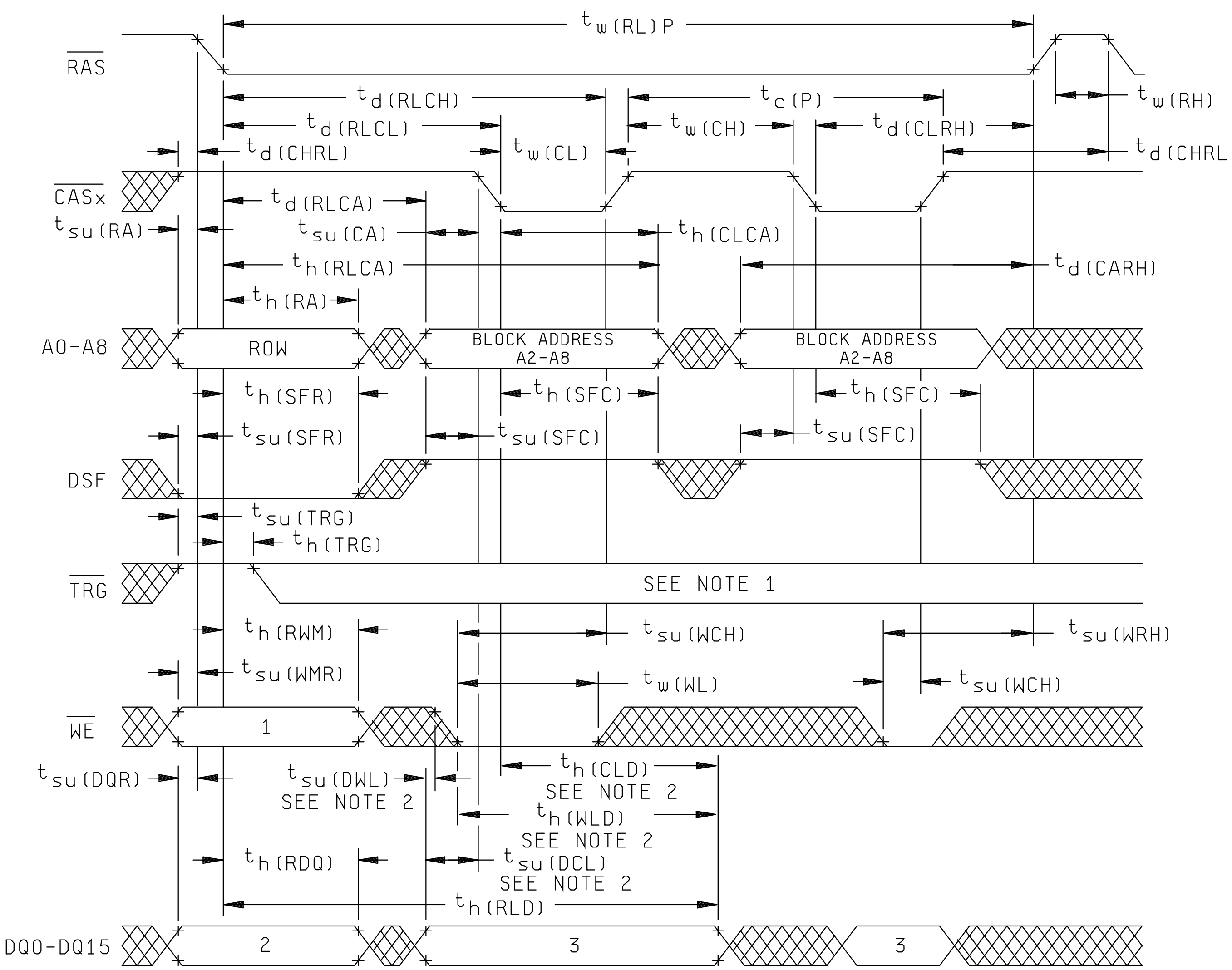


Cycle	State		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent w/B	L	Write mask	Column mask
Block-write operation with persistent w/B	L	Don't care	Column mask

For write-mask data, 0 = I/O write disable, 1 = I/O write enable.
For column-mask data (DQI to DQI + 3; I = 0, 4, 8, 12), 0 = column write disable, 1 = column write enable.

FIGURE 4. Timing waveforms - continued.

ENHANCED-PAGE-MODE BLOCK-WRITE-CYCLE TIMING



Cycle	State		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent w/B	L	Write mask	Column mask
Block-write operation with persistent w/B	L	Don't care	Column mask

For write-mask data, 0 = I/O write disable, 1 = I/O write enable.
For column-mask data (DQI to DQI + 3; I = 0, 4, 8, 12), 0 = column write disable, 1 = column write enable.

NOTES:

1. To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late-write feature is used. If the early-write cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.
2. Referenced to the first falling edge of $\overline{CAS}$ or the falling edge or $\overline{WE}$, whichever occurs later.

FIGURE 4. Timing waveforms - continued.

RAS -only refresh-cycle timing

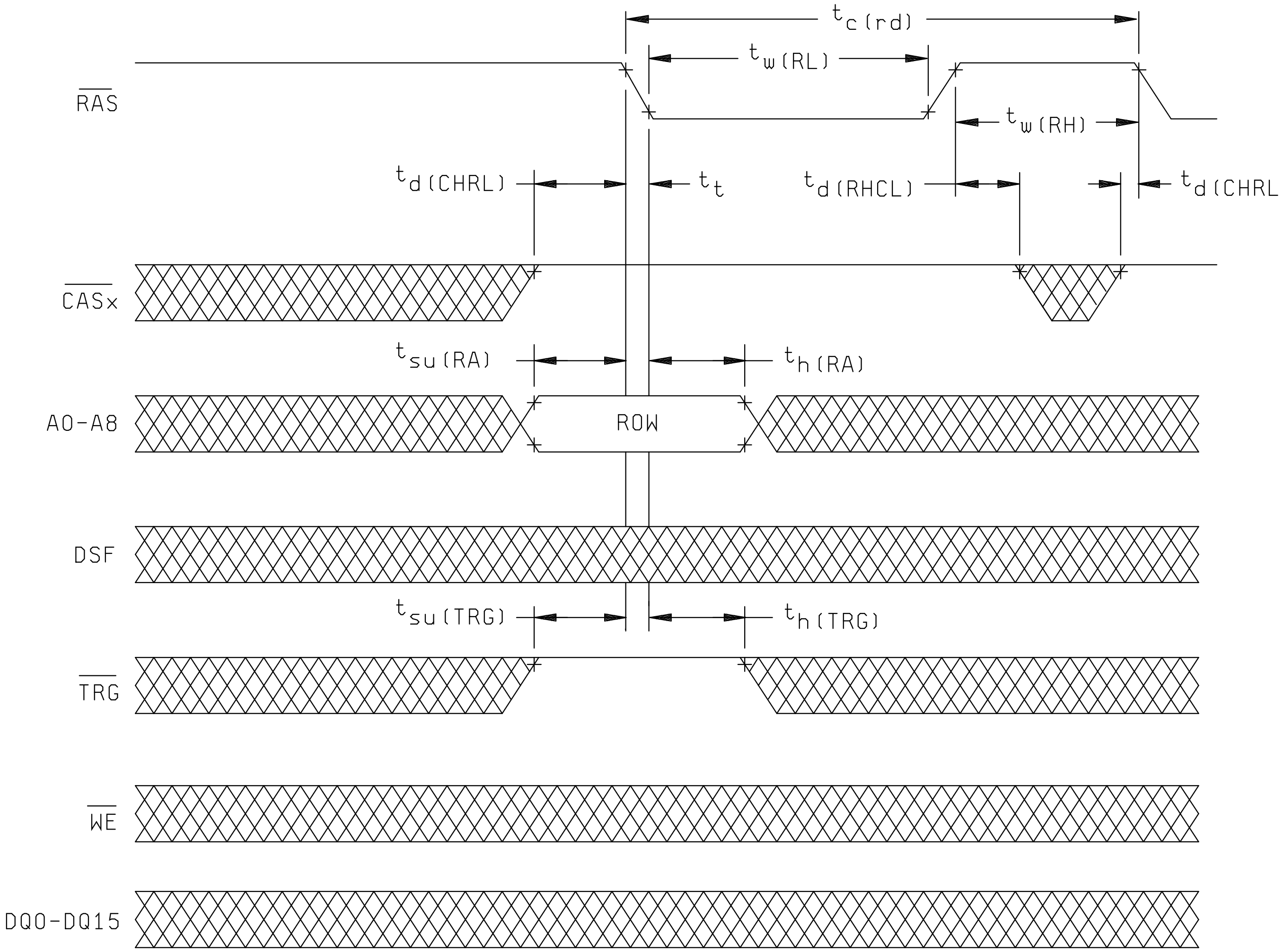
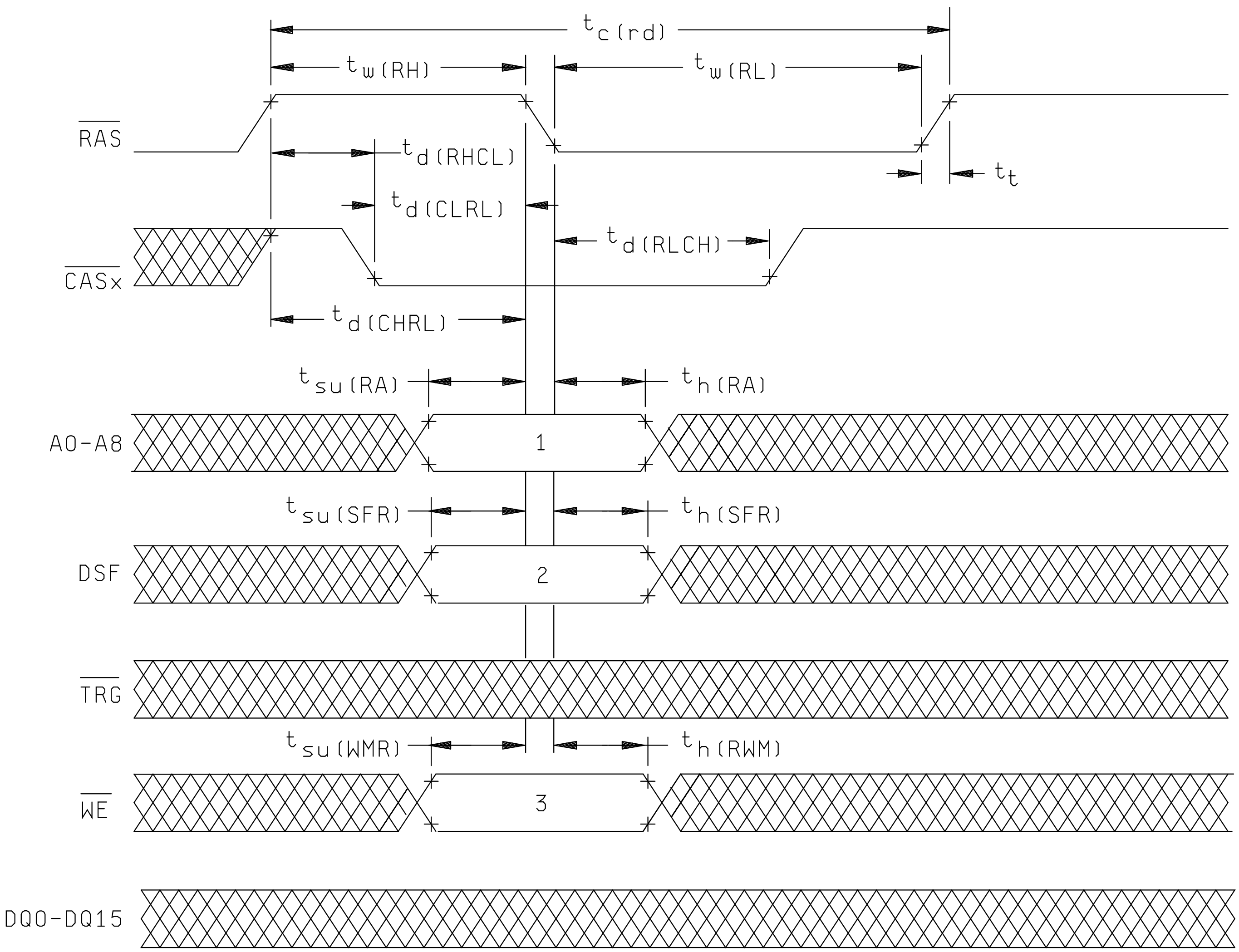


FIGURE 4. Timing waveforms - continued.

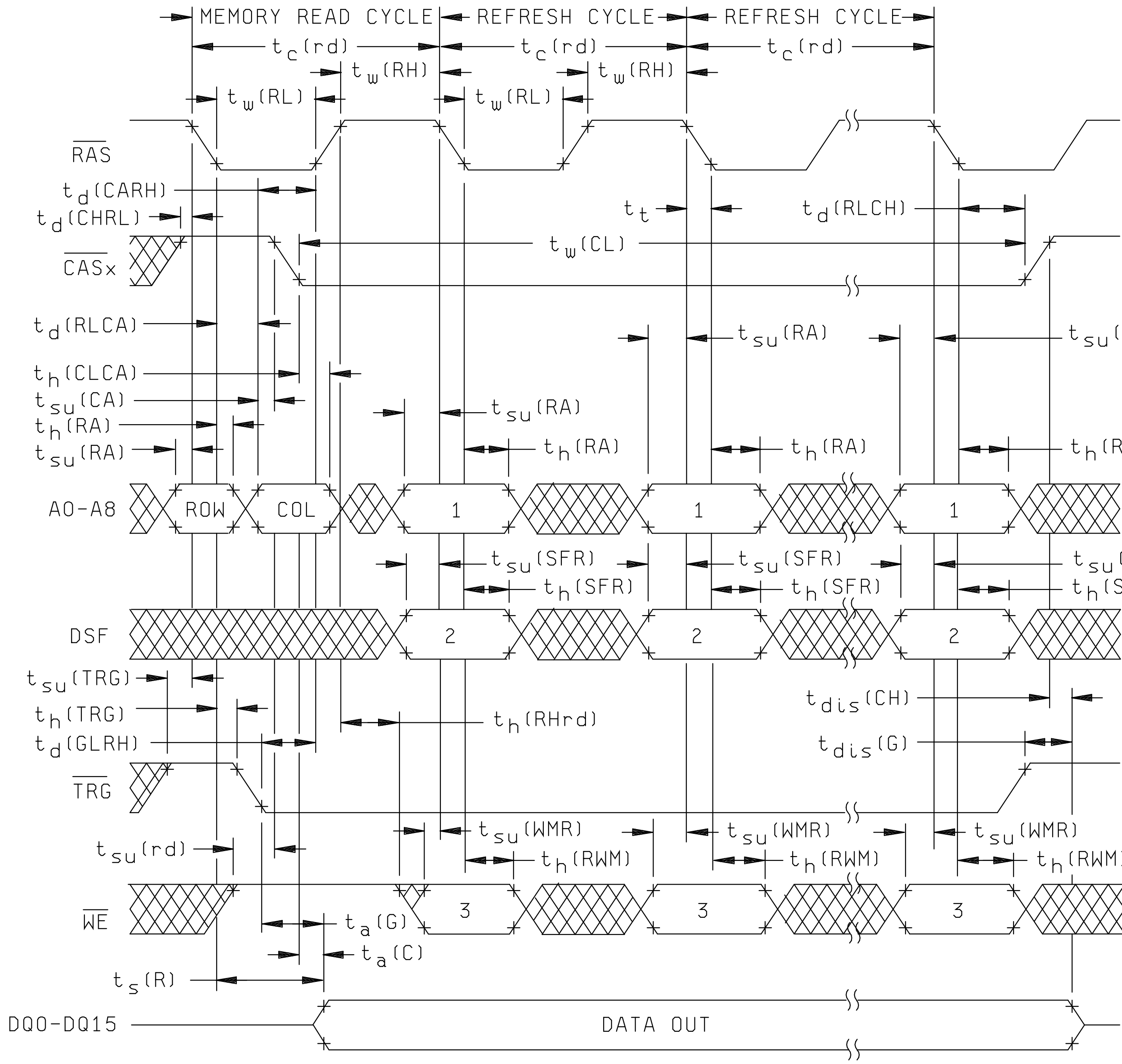
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH- CYCLE TIMING



Cycle	State		
	1	2	3
$\overline{CAS}$ -before- $\overline{RAS}$ refresh with option reset	Don't care	L	H
$\overline{CAS}$ -before- $\overline{RAS}$ refresh with no reset	Don't care	H	H
$\overline{CAS}$ -before- $\overline{RAS}$ refresh with stop-point set and no reset	Stop address	H	L

FIGURE 4. Timing waveforms - continued.

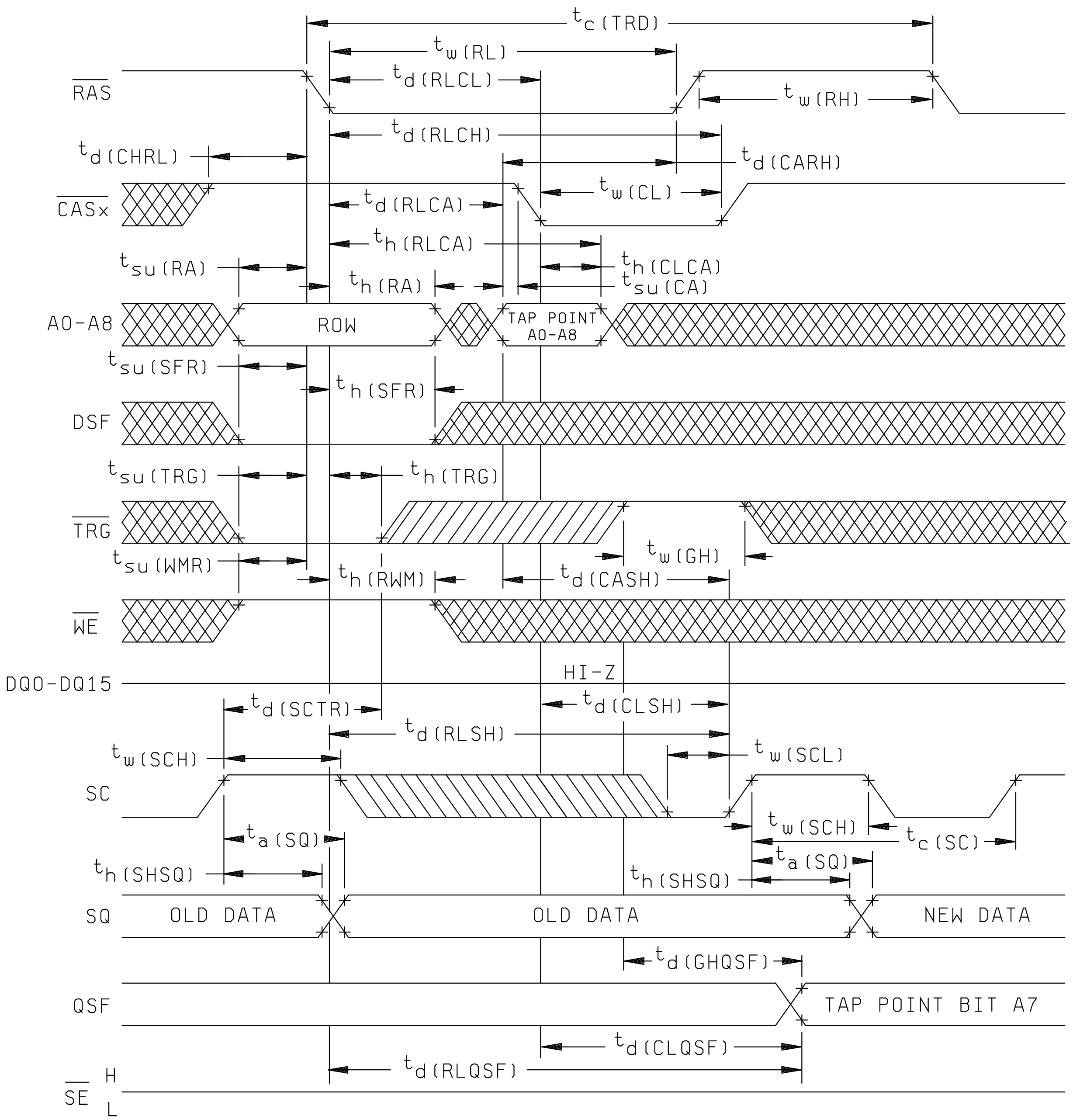
HIDDEN-REFRESH-CYCLE TIMING



Cycle	State		
	1	2	3
$\overline{CAS}$ -before- $\overline{RAS}$ refresh with option reset	Don't care	L	H
$\overline{CAS}$ -before- $\overline{RAS}$ refresh with no reset	Don't care	H	H
$\overline{CAS}$ -before- $\overline{RAS}$ refresh with stop-point set and no reset	Stop address	H	L

FIGURE 4. Timing waveforms - continued.

FULL-REGISTER TRANSFER READ TIMING, EARLY-LOAD OPERATIONS

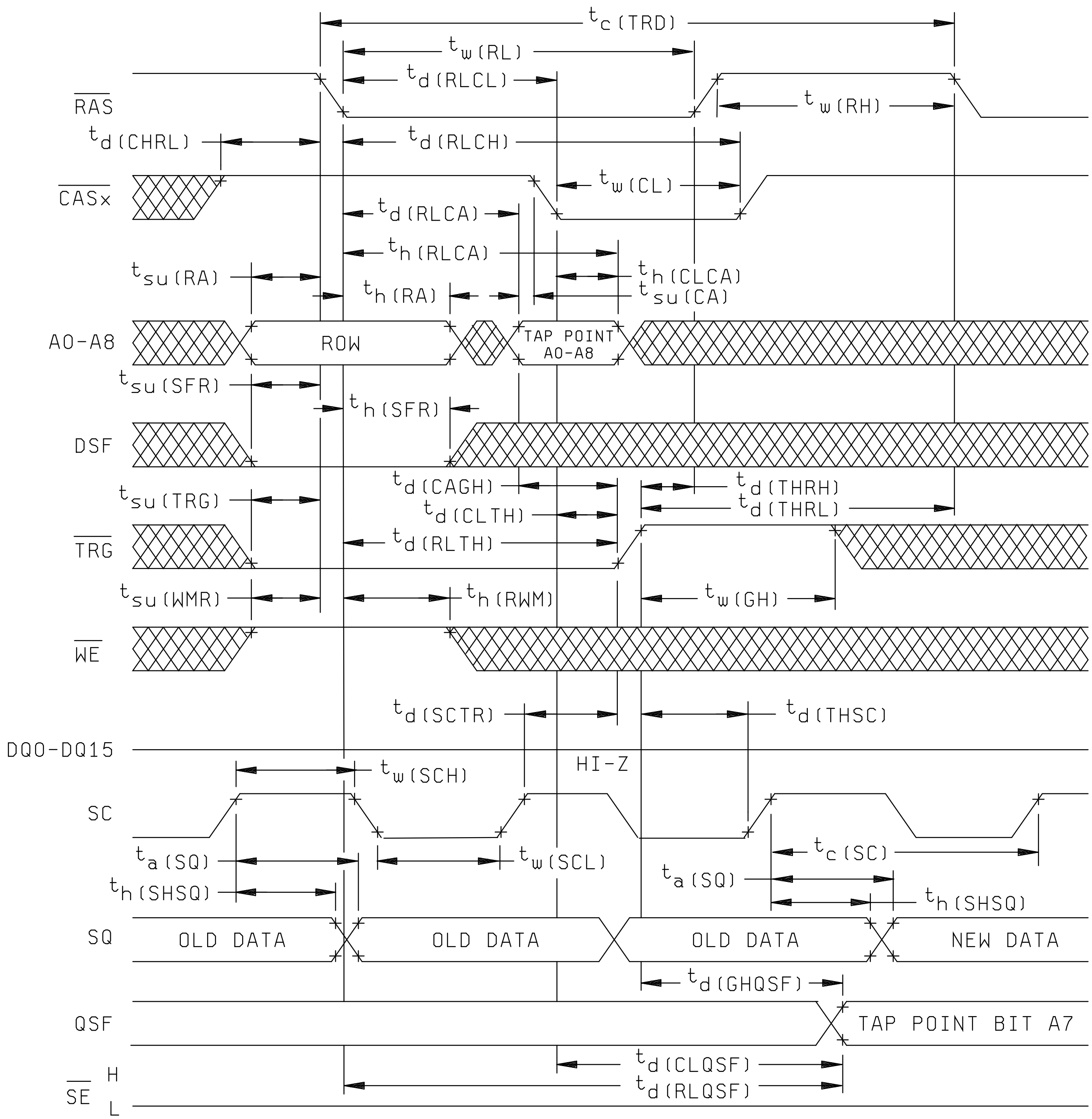


NOTES:

1. DQ outputs remain in the high-impedance state for the entire memory-to-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.
2. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to read from the data register after TRG has gone high must be activated by a positive transition of SC.
3. A0-A7: register tap point; A8: identifies the half of the transferred row.
4. Early-load operation is defined as $t_{h(TRG)}$ min < $t_{h(TRG)}$ < $t_{d(RLTH)}$ min.

FIGURE 4. Timing waveforms - continued.

FULL-REGISTER TRANSFER READ TIMING, REAL-TIME-LOAD OPERATION/LATE-LOAD OPERATION

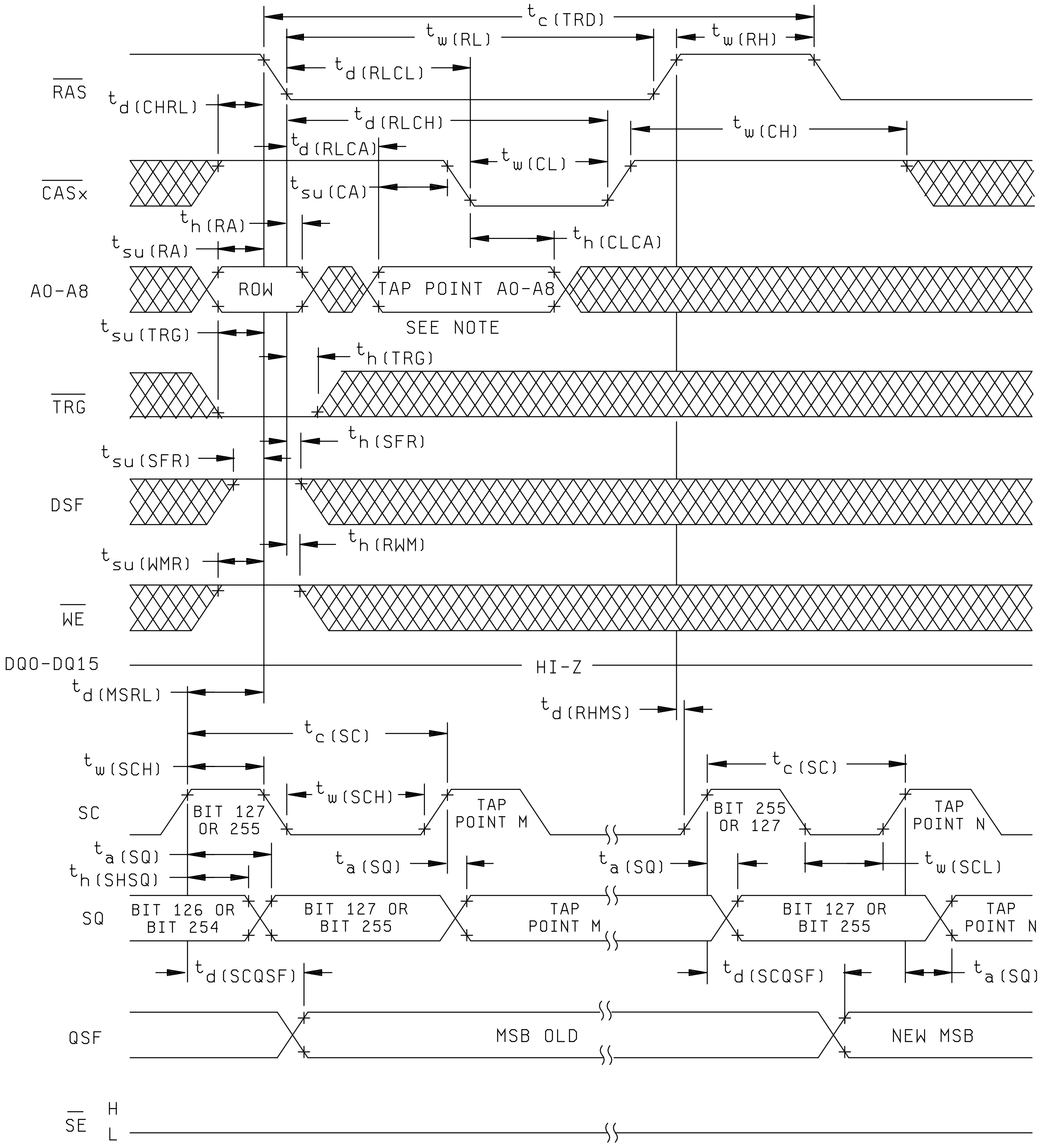


NOTES:

1. DQ outputs remain in the high-impedance state for the entire memory-to-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.
2. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to read from the data register after TRG has gone high must be activated by a positive transition of SC.
3. A0-A7: register tap point; A8: identifies the half of the transferred row.
4. Late-load operation is defined as $t_{d(THRH)} < 0$ ns.

FIGURE 4. Timing waveforms - continued.

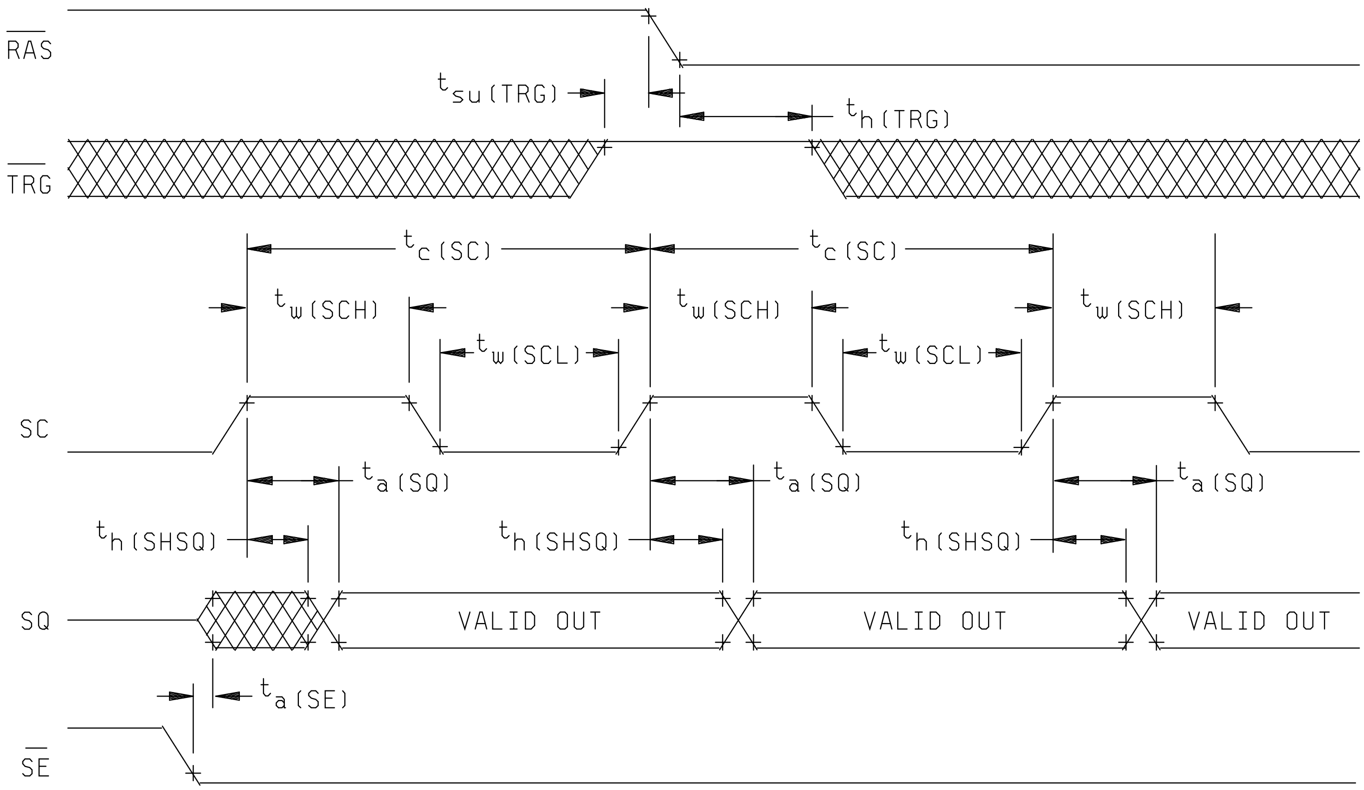
SPLIT-REGISTER TRANSFER READ TIMING



NOTE: A0-A6: tap point or the given half; A7: don't care; A8: identifies the DRAM row half.

FIGURE 4. Timing waveforms - continued.

Serial-read-cycle timing ($\overline{SE}$ = V_{IL})



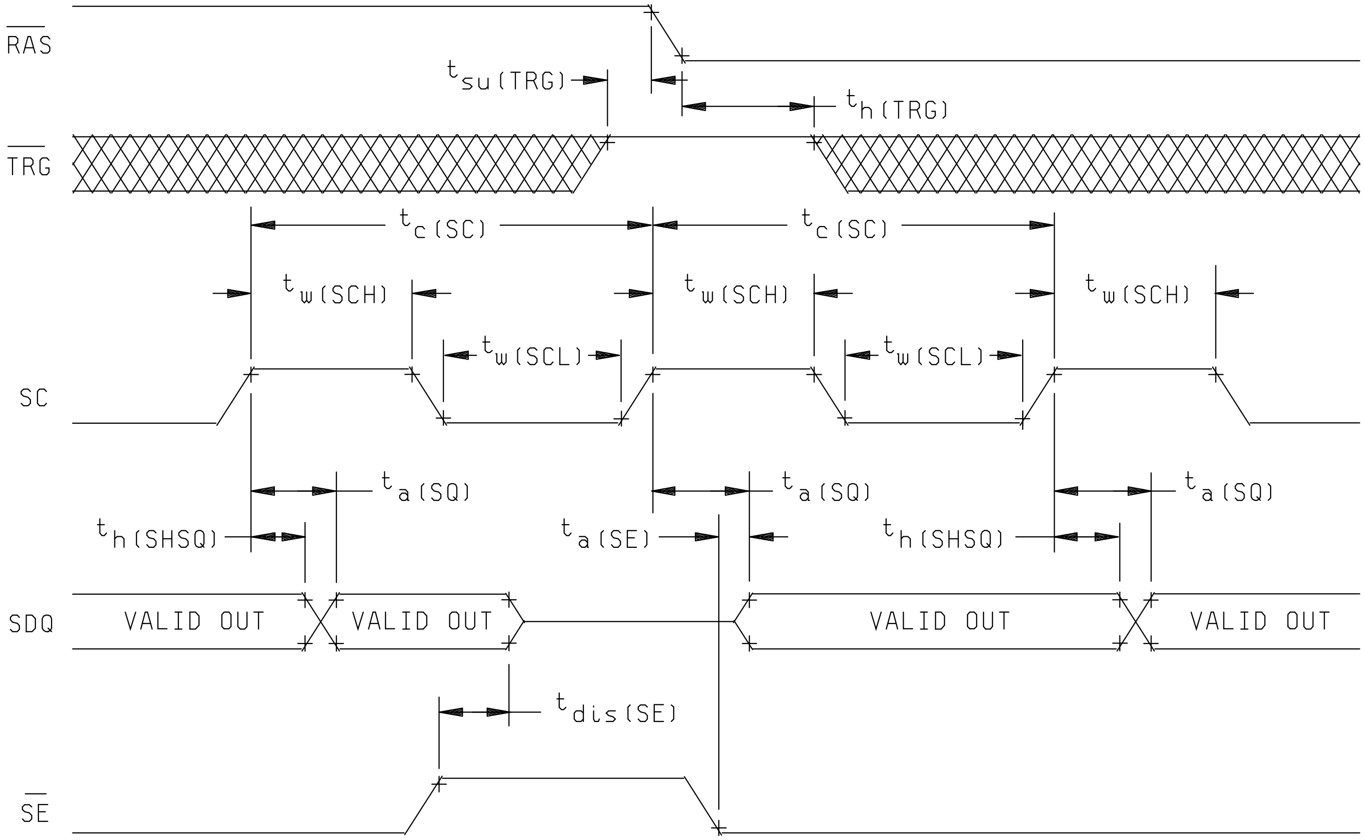
NOTES:

1. While the data is being read through the serial-data register, $\overline{TRG}$ is a don't care, except $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data transfer operation.

2. The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle.

FIGURE 4. Timing waveforms - continued.

Serial-read timing ($\overline{SE}$ -controlled read)



NOTES:

1. While the data is being read through the serial-data register, $\overline{TRG}$ is a don't care, except $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data transfer operation.

2. The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle.

FIGURE 4. Timing waveforms - continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preborn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Test 1/	Device types
	All
I_{LI}	±10% of specified value in table I
I_{LO}	±10% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

APPENDIX A

Appendix A forms a part of SMD 5962-94549

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Output high impedance (t_{OFF}). This pattern verifies the output buffer switches to high impedance (three-state) within the specified t_{OFF} after the rise of $\overline{CAS}$. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load address location with data.
Step 3: Raise $\overline{CAS}$ and read address location and guarantee $V_{OL} < V_{OUT} < V_{OH}$ after t_{OFF} delay.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 V_{CC} slew. This pattern indicates sense amplifier margin by slewing the supply voltage between memory writing and reading. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data with V_{CC} at 4.5 V.
Step 3: Change V_{CC} to 5.5 V.
Step 4: Read memory with background data.
Step 5: Load memory with background data complement.
Step 6: Change V_{CC} to 4.5 V.
Step 7: Read memory with background data complement.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 March data. This pattern tests for address uniqueness and multiple selections. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Read location 0.
Step 4: Write data complement in location 0.
Step 5: Repeat steps 3 and 4 for all other locations in the memory (sequentially).
Step 6: Read data complement in maximum address location.
Step 7: Write data in maximum address location.
Step 8: Repeat steps 6 and 7 for all other locations in the memory from maximum to minimum address.
Step 9: Read data in maximum address location.
Step 10: Write data complement in maximum address location.
Step 11: Repeat steps 6 and 7 for all other locations in the memory from maximum to minimum address.
Step 12: Read memory with data complement.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 Refresh test (cell retention) +125°C only. This test is used to check the retention time of the memory cells. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Pause t_{REF} (stop all clocks).
Step 4: Read memory with background data.
Step 5: Repeat steps 2 through 4 with data complement.

A.3.5 Algorithm E (pattern 5).

A.3.5.1 Read-modify-write (RMW). This pattern verifies the Read-modify-write mode for the memory. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Read memory with data and load with data complement using RMW cycle.
Step 4: Repeat step 3 for all address locations.
Step 5: Repeat steps 2 and 3 using data complement.

A.3.6 Algorithm F (pattern 6).

A.3.6.1 Page mode. This pattern verifies the Page mode for the memory. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load first page of memory with background data using Page mode cycle.
Step 3: Read first page of memory with data and load with data complement using Page mode cycle.
Step 4: Read first page of memory with data complement and load with data using Page mode cycle.
Step 5: Repeat steps 2 through 4 for remaining memory locations.

A.3.7 Algorithm G (pattern 7).

A.3.7.1 $\overline{CAS}$-before $\overline{RAS}$ refresh test. This test is used to verify the functionality of the $\overline{CAS}$-before $\overline{RAS}$ mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Perform 1024 $\overline{CAS}$-before $\overline{RAS}$ cycles while attempting to modify data.
Step 4: Read memory with background data.

A.3.8 Algorithm H (pattern 8).

A.3.8.1 $\overline{RAS}$-only refresh test. This test is used to verify the functionality of the $\overline{RAS}$-only mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Perform 1024 $\overline{RAS}$-only cycles while attempting to modify data.
Step 4: Repeat step 3 for 1 second.
Step 5: Read memory with background data.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-10-07

Approved sources of supply for SMD 5962-94549 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9454901MXA	3/	SMJ55161-80GBM
5962-9454901MYC	3/	SMJ55161-80HKCM
5962-9454902MXX	3/	SMJ55161-70GBM
5962-9454902MYX	3/	SMJ55161-70HKCM
5962-9454903QXA	3/	SMJ55161-75GBM
5962-9454903QYC	3/	SMJ55161-75HKCM

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply. The last known source is listed below.

Vendor CAGE number	Vendor name and address
0EU86	Austin Semiconductor Inc. Micross Components 8701 Cross Park Drive Suite 105 Austin, TX 78754-4566